ACPL-P346 and ACPL-W346

2.5 Amp Output Current Power & SiC MOSFET Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO6

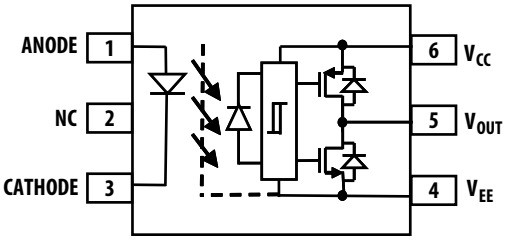
AVAGO TECHNOLOGIES

Data Sheet

Description

The ACPL-P346/W346 contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power and SiC(Silicon Carbide) MOSFETs used in inverter or AC-DC/DC-DC converter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving MOSFETs at high frequency for high efficiency conversion. The ACPL-P346 and ACPL-W346 have the highest insulation voltage of V_{IORM}= 891Vpeak and V_{IORM}= 1140V_{peak} respectively in the IEC/ EN/DIN EN 60747-5-5.

Functional Diagram



Note: A 1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_{EE}$ "POSITIVE GOING" (i.e., TURN-ON)	$V_{CC} - V_{EE}$ "NEGATIVE GOING" (i.e., TURN-OFF)	V_O
OFF	0 - 20 V	0 – 20 V	LOW
ON	0 – 8.1 V	0 – 7.1 V	LOW
ON	8.1 – 9.1 V	7.1 – 8.1 V	TRANSITION
ON	9.1 – 20V	8.1 – 20 V	HIGH

Features

- 2.5 A maximum peak output current
- 2.0 A minimum peak output current
- Rail-to-rail output voltage
- 120 ns maximum propagation delay
- 50 ns maximum propagation delay difference
- LED current input with hysteresis
- 50 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- I_{CC} = 4.0 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating V_{CC} Range: 10 to 20 V
- Industrial temperature range: -40 °C to 105 °C
- Safety Approval
  - UL Recognized 3750/5000 V_{RMS} for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 891/1140 V_{peak}

Applications

- Power and SiC MOSFET gate drive
- AC and Brushless DC motor drives
- Switching power supplies

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-P346 is UL Recognized with 3750 V_{RMS} for 1 minute per UL1577.

ACPL-W346 is UL Recognized with 5000 V_{RMS} for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape& Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-P346 ACPL-W346	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P346-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

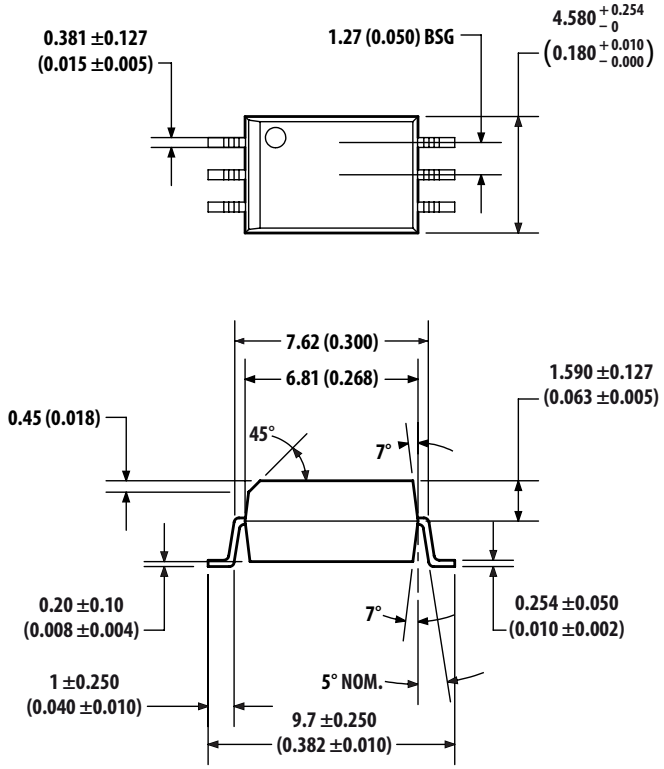
Example 2:

ACPL-W346-000E to order product of Stretched SO-6 Surface Mount package in Tube packaging and RoHS compliant.

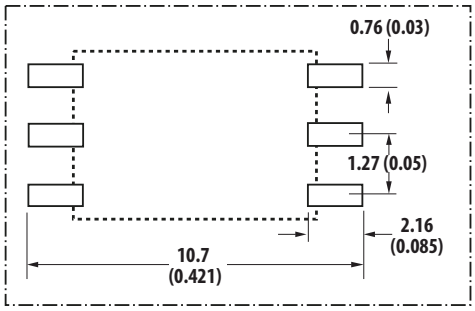
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

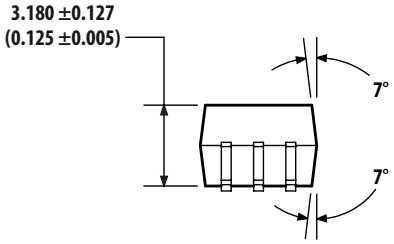
Package Outline Drawings

ACPL-P346 Stretched SO-6 Package (7 mm clearance)



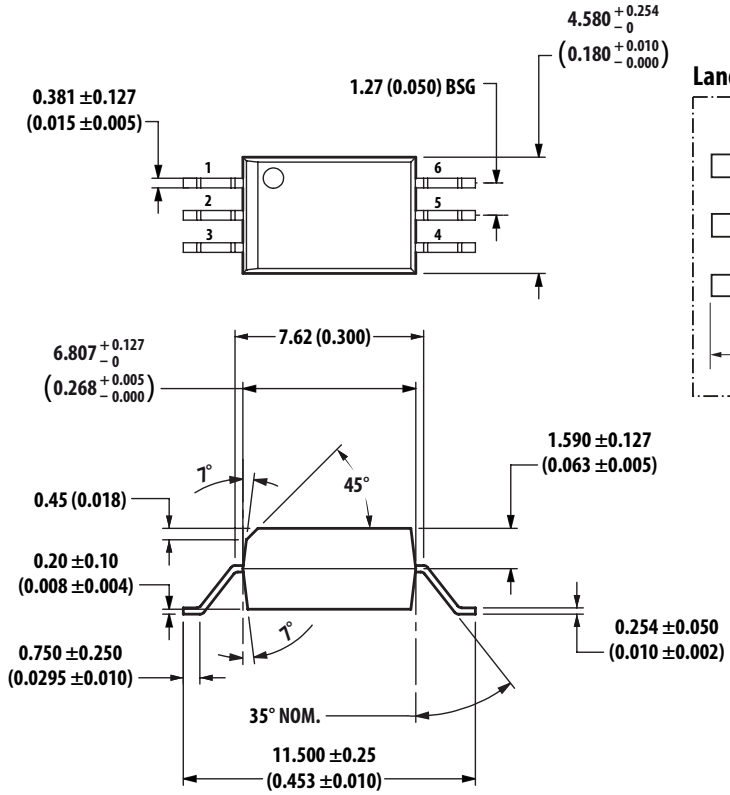
Land Pattern Recommendation



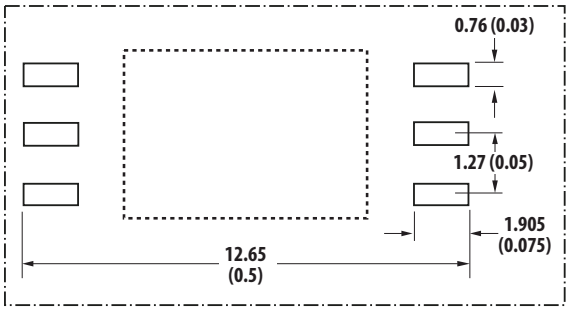


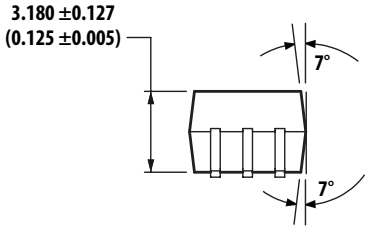
Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)

ACPL-W346 Stretched SO-6 Package (8 mm clearance)



Land Pattern Recommendation





Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-P346/W346 is approved by the following organizations:

UL	Recognized under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} (ACPL-P346) and V_{ISO} = 5000 V_{RMS} (ACPL-W346).
CSA	CSA Component Acceptance Notice #5, File CA 88324
IEC/EN/DIN EN 60747-5-5 (Option 060 Only)	Maximum Working Insulation Voltage V_{IORM} = 891V_{peak} (ACPL-P346) and V_{IORM} = 1140 V_{peak}(ACPL-W346)

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060)

Description	Symbol	ACPL-P346 Option 060	ACPL-W346 Option 060	Unit
Installation classification per DIN VDE 0110/39, Table 1				
for rated mains voltage ≤ 150 Vrms		I – IV	I – IV	
for rated mains voltage ≤ 300 Vrms		I – IV	I – IV	
for rated mains voltage ≤ 450 Vrms		I – III	I – IV	
for rated mains voltage ≤ 600 Vrms		I – III	I – IV	
for rated mains voltage ≤ 1000 Vrms			I – III	
Climatic Classification		40/105/21	40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with tm=1 sec, Partial discharge < 5 pC	V_{PR}	1671	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, tm=10 sec, Partial discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage tini = 60 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	TS	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at TS, V_{IO} = 500 V	RS	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P346	ACPL-W346	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Notes:
1. All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 μs pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Total Output Supply Voltage	(V_{CC} - V_{EE})	0	25	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
eOutput IC Power Dissipation	P_O		500	mW	3
Total Power Dissipation	P_T		550	mW	4

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Max.	Units	Note
Operating Temperature	T_A	- 40	105	°C	
Output Supply Voltage	(V_{CC} - V_{EE})	10	20	V	
Input Current (ON)	$I_{F(ON)}$	7	11	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	

Table 5. Electrical Specifications (DC)

All typical values are at T_A = 25 °C, V_{CC} - V_{EE} = 10 V, V_{EE} = Ground. All minimum and maximum specifications are at recommended operating conditions (T_A = -40 to 105 °C, $I_{F(ON)}$ = 7 to 11 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{EE} = Ground , V_{CC} = 10 to 20 V), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	I_{OH}	-2.0	-3.4		A	V_{CC} – V_O = 10 V	3, 4	5
Low Level Peak Output Current	I_{OL}	2.0	4.4		A	V_O - V_{EE} = 10 V	6, 7	5
High Output Transistor RDS(ON)	$R_{DS,OH}$	0.3	1.7	3.5	Ω	I_{OH} = -2.0 A	8	6
Low Output Transistor RDS(ON)	$R_{DS,OL}$	0.3	0.7	2.0	Ω	I_{OL} = 2.0 A	9	6
High Level Output Voltage	V_{OH}	Vcc-0.3	Vcc – 0.2		V	I_O = -100 mA, I_F = 9 mA	2, 4	7, 8
High Level Output Voltage	V_{OH}		Vcc		V	I_O = 0 mA, I_F = 9 mA	1	
Low Level Output Voltage	V_{OL}		0.1	0.25	V	I_O = 100 mA	5, 7	
High Level Supply Current	I_{CCH}		2.6	4.0	mA	I_F = 9 mA	10, 11	
Low Level Supply Current	I_{CCL}		2.6	4.0	mA	V_F = 0V		
Threshold Input Current Low to High	I_{FLH}	0.5	1.5	4.0	mA	V_O > 5 V	12, 13	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 9 mA	19	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.7		mV/°C			
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 100 μA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	8.1	8.6	9.1	V	V_O > 5 V, I_F = 9 mA		
	V_{UVLO-}	7.1	7.6	8.1				
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0		V			

Table 6. Switching Specifications (AC)

All typical values are at T_A = 25 °C, V_{CC} - V_{EE} = 10 V, V_{EE} = Ground. All minimum and maximum specifications are at recommended operating conditions (T_A = -40 to 105 °C, $I_{F(ON)}$ = 7 to 11 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{EE} = Ground), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	30	55	120	ns	Rg = 10 Ω, Cg = 10 nF, f = 200 kHz , Duty Cycle = 50%, V_{CC} = 10V	14, 15, 16, 17	
Propagation Delay Time to Low Output Level	t_{PHL}	30	55	120	ns			
Pulse Width Distortion	PWD		0	50	ns			9
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-50		50	ns		24, 25	10
Propagation Delay Skew	t_{PSK}			40	ns			11
Rise Time	t_R		8	30	ns	Cg = 1 nF, f = 200 kHz , Duty Cycle = 50%, V_{CC} = 10V	18, 20	
Fall Time	t_F		8	30	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50	70		kV/µs	T_A = 25 °C, I_F = 9 mA, V_{CC} = 20 V, V_{CM} = 1500 V with split resistors	21	12, 13
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50	70		kV/µs	T_A = 25°C, V_F = 0 V, V_{CC} = 20 V, V_{CM} = 1500 V with split resistors		14, 15

Table 7. Package Characteristics

All typical values are at T_A = 25 °C. All minimum/maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	ACPL-P346	3750			V_{RMS}	RH < 50%, t = 1 min., T_A = 25 °C		15,17
		ACPL-W346	5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25 °C		16,18
Input-Output Resistance	R_{I-O}			$>50^{12}$		Ω	V_{I-O} = 500 V_{DC}		17
Input-Output Capacitance	C_{I-O}			0.6		pF	f =1 MHz		
LED-to-Ambient Thermal Resistance	R_{11}			135		°C/W			18
LED-to-Detector Thermal Resistance	R_{12}			27					
Detector-to-LED Thermal Resistance	R_{21}			39					
Detector-to-Ambient Thermal Resistance	R_{22}			47					

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:
1. Derate linearly above 85 °C free-air temperature at a rate of 0.3 mA/ °C.
2. Maximum pulse width = 10 µs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 85 °C free-air temperature at a rate of 12.5 mW/ °C .
4. Derate linearly above 85 °C free-air temperature at a rate of 13.75 mW/ °C. The maximum LED junction temperature should not exceed 125 °C.
5. Maximum pulse width = 10 µs.
6. Output is sourced at -2.0 A/2.0 A with a maximum pulse width = 10 µs.
7. In this test V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
8. Maximum pulse width = 1 ms.
9. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
10. The difference between t_{PHL} and t_{PLH} between any two ACPL-P346 parts under the same test condition.
11. t_{PSK} is equal to the worst case diff erence in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
12. Pin 2 needs to be connected to LED common. Split resistor network in the ratio 1.5:1 with 232 Ω at the anode and 154 Ω at the cathode.
13. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_O > 10.0$ V).
14. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_O < 1.0$ V).
15. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
16. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
17. Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5 and 6 shorted together.
18. The device was mounted on a high conductivity test board as per JEDEC 51-7.

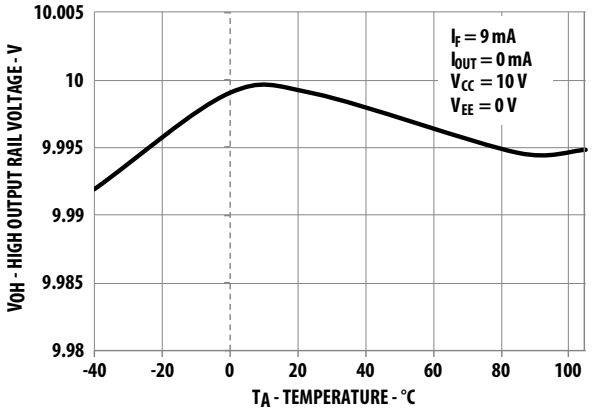


Figure 1. High output rail voltage vs. temperature.

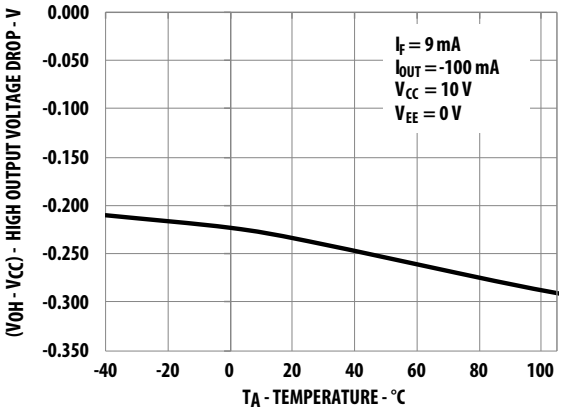


Figure 2. V_{OH} vs. temperature.

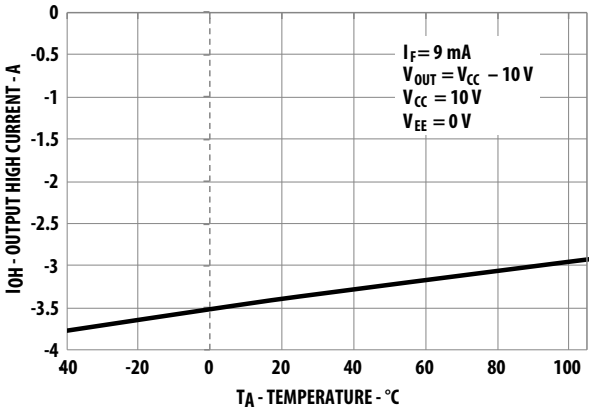


Figure 3. I_{OH} vs. temperature.

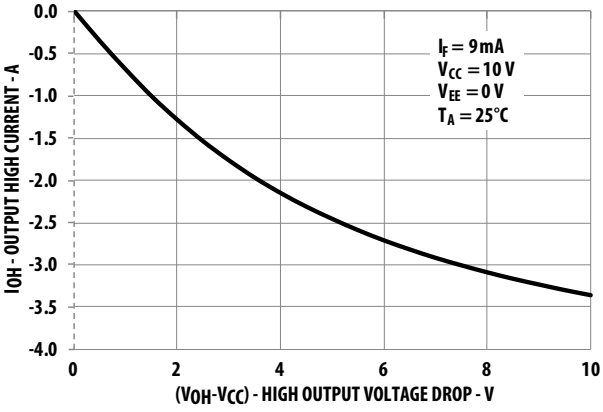


Figure 4. I_{OH} vs. V_{OH}.

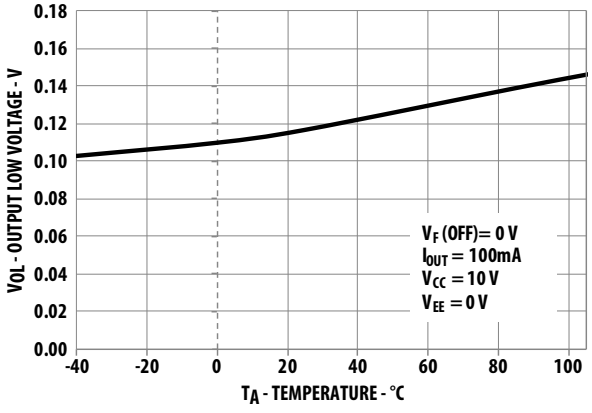


Figure 5. V_{OL} vs. Temperature.

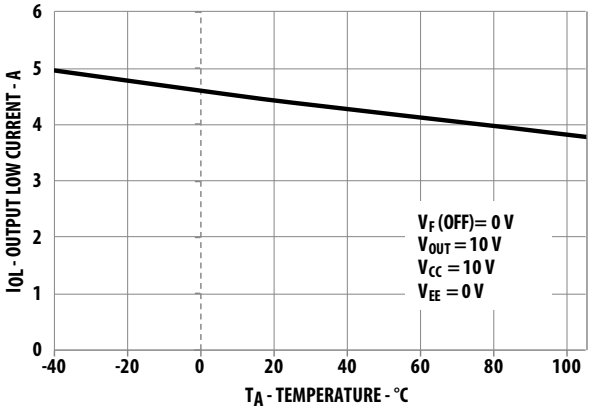


Figure 6. I_{OL} vs. temperature.

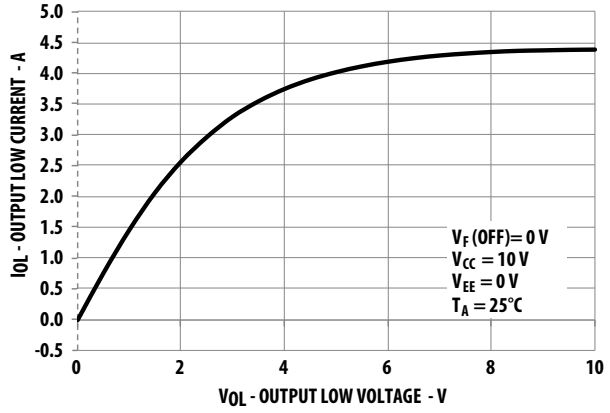


Figure 7. I_{OL} vs. V_{OL}.

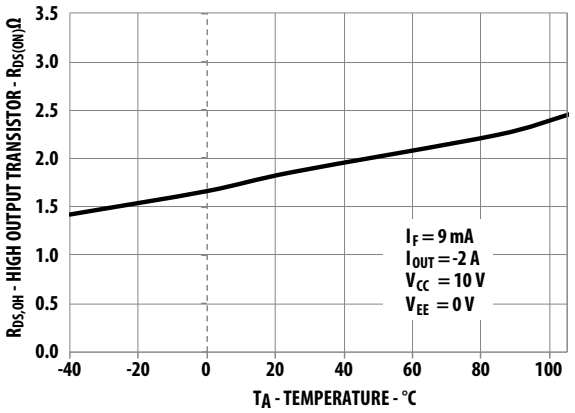


Figure 8. $R_{DS,OH}$ vs. temperature.

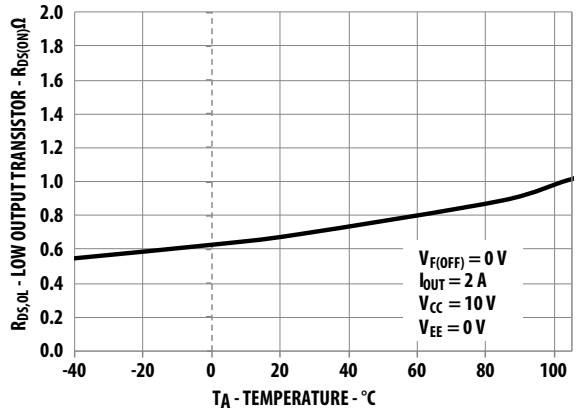


Figure 9. $R_{DS,OL}$ vs. temperature.

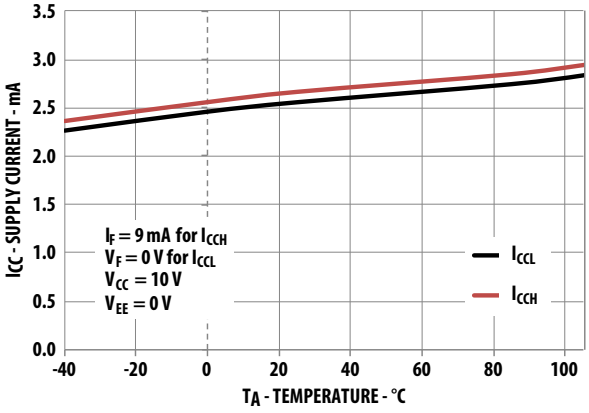


Figure 10. I_{CC} vs. temperature.

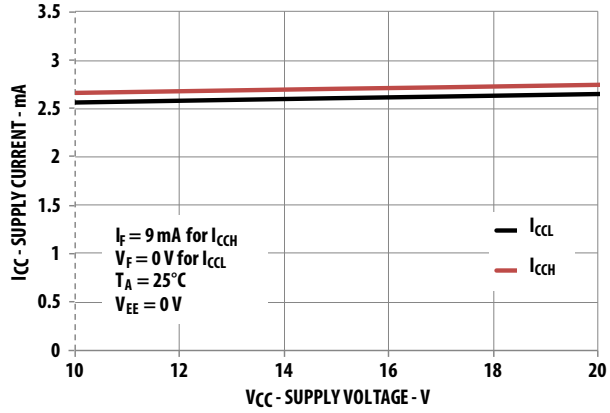


Figure 11. I_{CC} vs. V_{CC}.

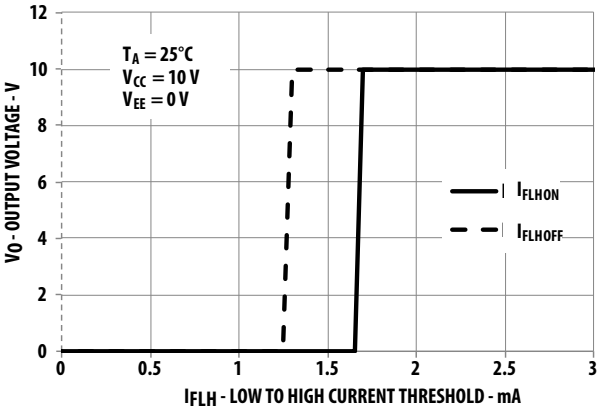


Figure 12. I_{FLH} hysteresis.

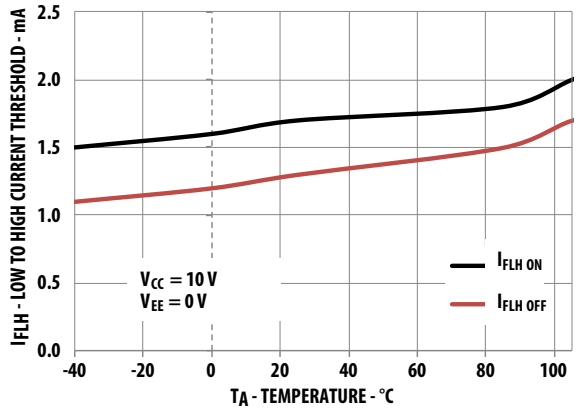


Figure 13. I_{FLH} vs. temperature.

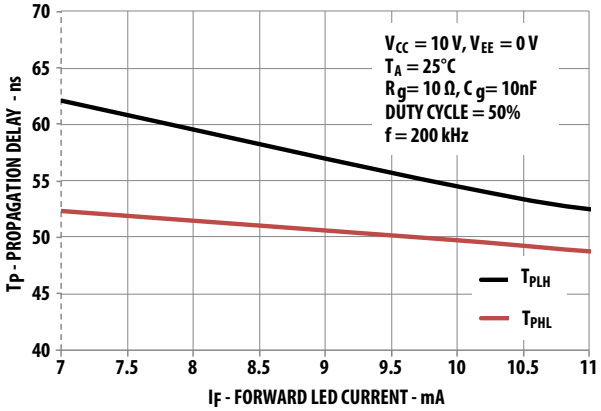


Figure 14. Propagation delay vs. I_F.

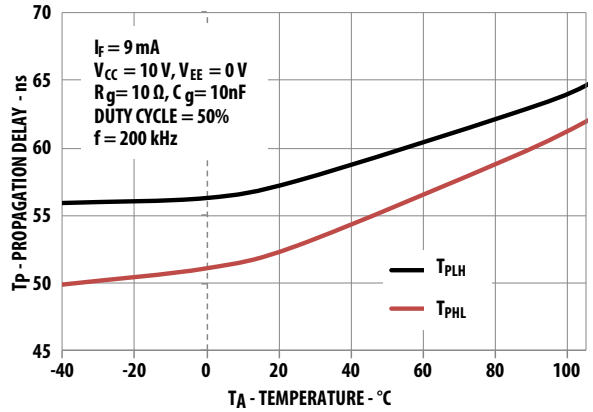


Figure 15. Propagation delay vs. temperature.

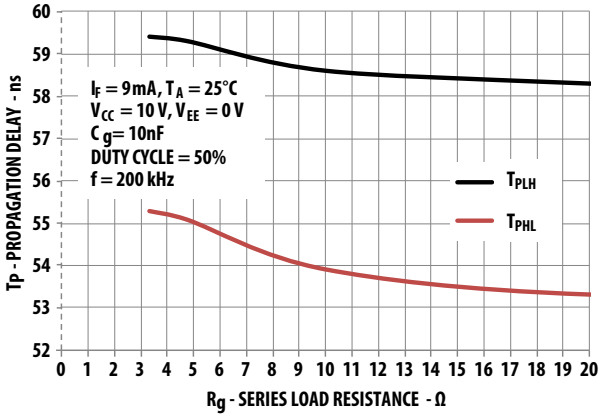


Figure 16. Propagation delay vs. Rg.

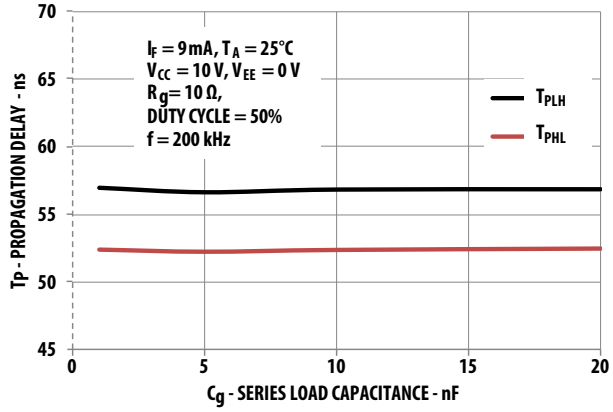


Figure 17. Propagation delay vs. Cg.

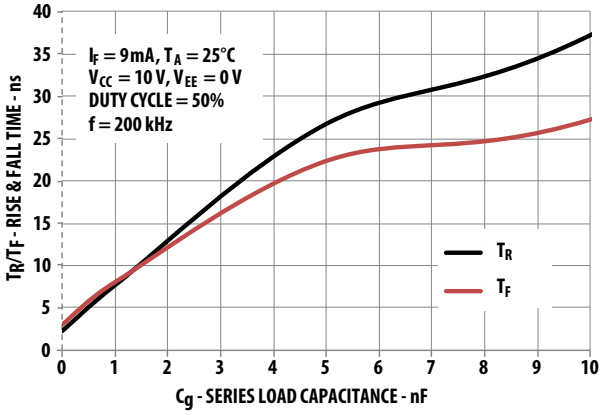


Figure 18. Rise & Fall time vs. Cg.

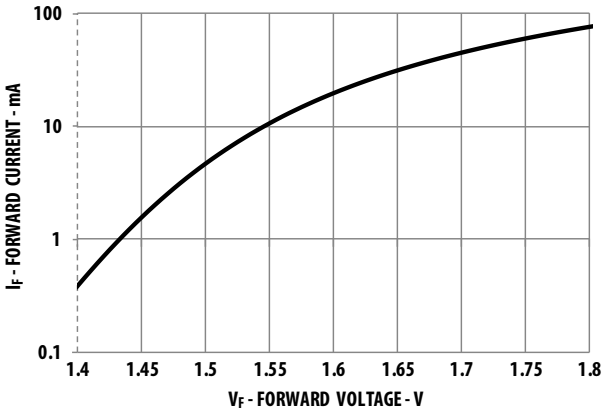
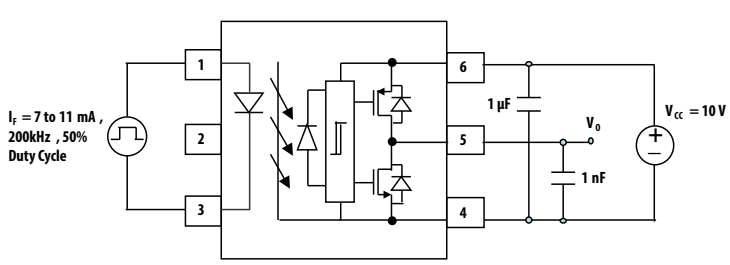


Figure 19. Input Current vs. forward voltage.



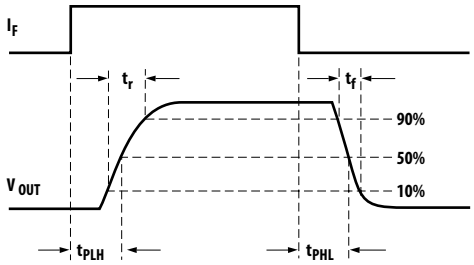
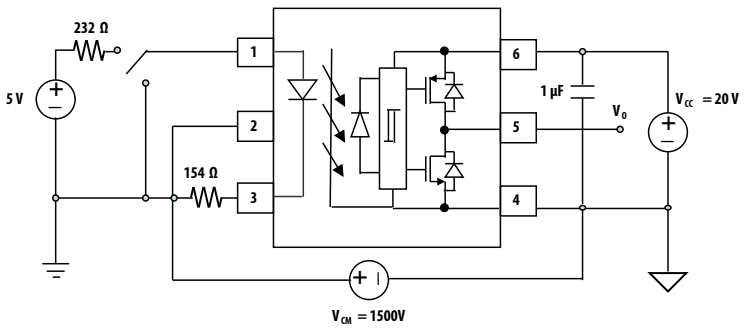


Figure 20. tr and tf test circuit and waveforms.



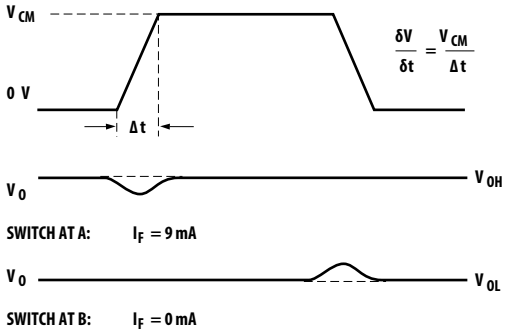


Figure 21. CMR test circuit with split resistors network and waveforms.

Application Information

Product Overview Description

The ACPL-P346/W346 is an optically isolated power output stage capable of driving power or SiC. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance and two times faster speed than the previous generation products.

The high peak output current and short propagation delay are needed for fast MOSFET switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the MOSFET's gate voltage is driven to the optimum intended level with no power loss across the MOSFET. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

It has very high CMR(common mode rejection) rating which allows the microcontroller and the MOSFET to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminates the need of additional Schmitt trigger circuit at the input LED.

The stretched SO6 package which is up to 50% smaller than conventional DIP package facilitates smaller and more compact design. These stretched packages are compliant to many industrial safety standards such as IEC/EN/DIN EN 60747-5-5, UL 1577 and CSA.

Recommended Application Circuit

The recommended application circuit shown in Figure 22 illustrates a typical gate drive implementation using the ACPL-P346.

The supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (4.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1.5:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor R_G serves to limit gate charge current and controls the MOSFET switching times.

In PC board design, care should be taken to avoid routing the MOSFET drain or source traces close to the ACPL-P346 input as this can result in unwanted coupling of transient signals into ACPL-P346 and degrade performance.

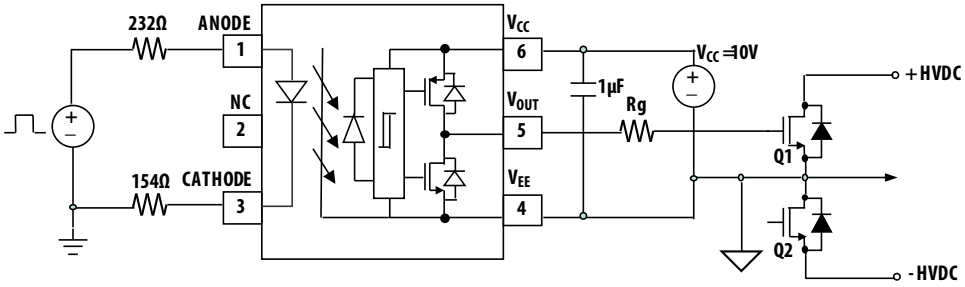


Figure 22. Recommended application circuit with split resistors LED.

Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The MOSFET and Rg in Figure 22 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-P346/W346.

$$Rg \geq \frac{V_{CC}-V_{EE}}{I_{OLPEAK}} - R_{DSON(MIN)}$$

$$= \frac{10-0V}{2.5A} - 0.3\Omega$$

$$= 3.7\Omega$$

The external gate resistor, Rg and internal minimum turn-on resistance, R_{DSON} will ensure the output current will not exceed the device absolute maximum rating of 2.5 A.

Step 1: Check the ACPL-P346/W346 power dissipation and increase Rg if necessary. The ACPL-P346/W346 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$

$P_E = I_F \cdot V_F \cdot$ Duty Cycle

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$

$= I_{CC} \cdot (V_{CC}\text{-}V_{EE}) + P_{HS} + P_{LS}$

$P_{HS} = (V_{CC}*Q_G*f) * R_{DS,OH(MAX)} / (R_{DS,OH(MAX)}+Rg) / 2$

$P_{LS} = (V_{CC}*Q_G*f) * R_{DS,OL(MAX)} / (R_{DS,OL(MAX)}+Rg) / 2$

Using I_F(worst case) = 11 mA, Rg = 3.7 Ω,
Max Duty Cycle = 80%, Q_G = 100 nC (650V 20A MOSFET),
f = 200 kHz and $T_{A\ max}$ = 85 °C:

$P_E = 11mA \cdot 1.95V \cdot 0.8 = 17mW$

$P_{HS} = (10V \cdot 100nC \cdot 200\ kHz) \cdot 3.5\Omega/(3.5\Omega+3.7\Omega)/2$

$= 48.6mW$

$P_{LS} = (10V \cdot 100nC \cdot 200\ kHz) \cdot 2.0\Omega/(2.0\Omega+3.7\Omega)/2$

$= 35.1mW$

$P_O = 4mA \cdot 10V + 48.6mW + 35.1mW$

$= 123.7mW < 500\ mW\ (P_{O(MAX)}$ @ 85 °C)

The value of 4 mA for I_{CC} in the previous equation is the maximum I_{CC} over the entire operating temperature range.

Since P_O is less than $P_{O(MAX)}$, Rg = 3.7 Ω is alright for the power dissipation.

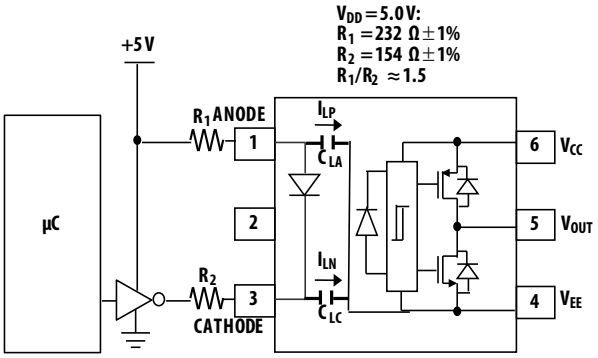


Figure 23. Recommended high-CMR drive circuit for the ACPL-P346/W346.

LED Drive Circuit Considerations for High CMR Performance

Figure 23 shows the recommended drive circuit for the ACPL-P346/W346 that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED's anode and cathode. Common-mode transients can be capacitive coupled from the LED anode, through C_{LA} (or cathode through C_{LC}) to the output-side ground causing current to be shunted away from the LED (which is not wanted when the LED should be on) or conversely cause current to be injected into the LED (which is not wanted when the LED should be off).

Table 8 shows the directions of I_{LP} and I_{LN} depend on the polarity of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CM_H, since the output is at "high" state) depends on LED current (I_F). For conditions where IF is close to the switching threshold (I_{FLH}), CM_H also depends on the extent to which I_{LP} and I_{LN} balance each other. In other words, any condition where a common-mode transient causes a momentary decrease in I_F (i.e. when $dV_{CM}/dt > 0$ and $|I_{LP}| > |I_{LN}|$, referring to Table 8) will cause a common-mode failure for transients which are fast enough.

Likewise for a common-mode transient that occurs when the LED is off (i.e. CM_L, since the output is at "low" state), if an imbalance between I_{LP} and I_{LN} results in a transient IF equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike above 1 V, which constitutes a CM_L failure. The balanced I_{LED}-setting resistors help equalize the common mode voltage change at the anode and cathode. The shunt drive input circuit will also help to achieve high CM_L performance by shunting the LED in the off state.

Table 8. Common Mode Pulse Polarity and LED current Transients

dV_{CM}/dt	I_{LP} Direction	I_{LP} Direction	If $\|I_{LP}\| < \|I_{LN}\|$, I_F is momentarily	If $\|I_{LP}\| > \|I_{LN}\|$, I_F is momentarily
Positive (>0)	Away from LED anode through C_{LA}	Away from LED cathode through C_{LC}	Increase	Decrease
Negative(<0)	Toward LED anode through C_{LA}	Toward LED cathode through C_{LC}	Decrease	Increase

Dead Time and Propagation Delay Specifications

The ACPL-P346/W346 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

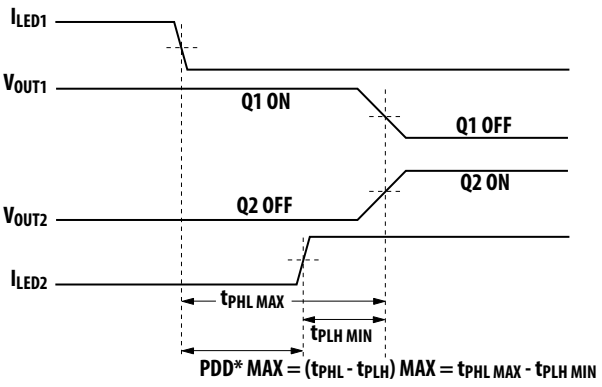
To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 24. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 100 ns over the operating temperature range of 40 °C to 105 °C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 25. The maximum dead time for the ACPL-P346/W346 is 100 ns (= 50 ns - (-50 ns)) over an operating temperature range of -40 °C to 105 °C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical MOSFETs.

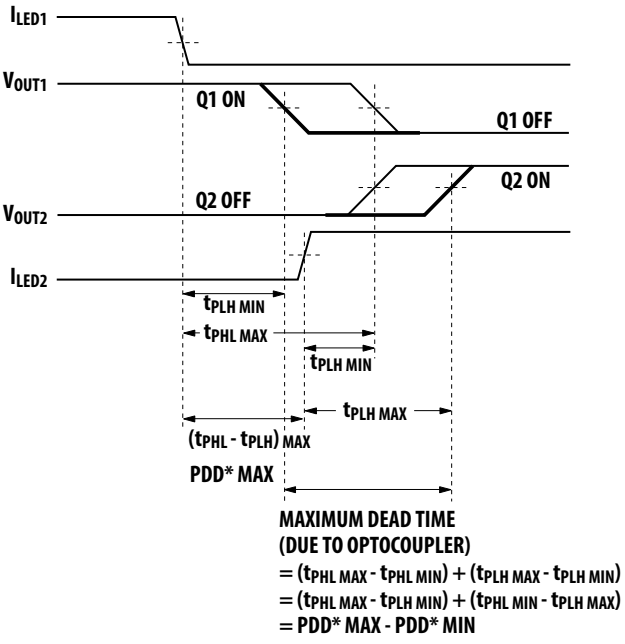
LED Current Input with Hysteresis

The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 12) provides differential mode noise immunity and minimizes the potential for output signal chatter.



*PDD = Propagation Delay Difference
Note: for PDD calculations the propagation delays
Are taken at the same temperature and test conditions.

Figure 24. Minimum LED skew for zero dead time



*PDD = Propagation Delay Difference
Note: For Dead Time and PDD calculations all propagation delays are taken at the same temperature and test conditions.

Figure 25. Waveforms for dead time

Thermal Model for ACPL-P346/W346 Stretched SO6 Package Optocoupler

Definitions:

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector / Output IC (W).

T_1: Junction temperature of LED (˚C).

T_2: Junction temperature of Detector (˚C).

Ta: Ambient temperature.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23 ˚C in still air

Thermal Resistance	°C/W
R_{11}	135
R_{12}	27
R_{21}	39
R_{22}	47

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$T_1 = (R_{11} * P_1 + R_{12} * P_2) + Ta$ -- (1)

$T_2 = (R_{21} * P_1 + R_{22} * P_2) + Ta$ -- (2)

Using the given thermal resistances and thermal model formula in this datasheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperatures should be within the absolute maximum rating.

For example, given P_1 = 17 mW, P_2 = 124 mW, Ta = 85 °C:

LED junction temperature,

$T_1 = (R_{11} * P_1 + R_{12} * P_2) + Ta$
$= (135 * 0.017 + 27 * 0.124) + 85$
$= 90.7$ °C

Output IC junction temperature,

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + Ta$
$= (39 * 0.017 + 47 * 0.124) + 85$
$= 91.5$ °C

T_1 and T_2 should be limited to 125 °C based on the board layout and part placement.

Related Documents

AV02-0421EN	Application Note 5336	Gate Drive Optocoupler Basic Design for IGBT / MOSFET
AV02-3698EN	Application Note 1043	Common-Mode Noise: Sources and Solutions
AV02-0310EN	Reliability Data	Plastics Optocouplers Product ESD and Moisture Sensitivity

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-4078EN - May 10, 2013