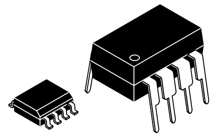


SLUS515 –SEPTEMBER 2002

TRANSITION MODE PFC CONTROLLER

FEATURES

- Transition Mode PFC Controller for Low Implementation Cost
- Industry Pin Compatibility With Improved Feature Set
- Improved Transient Response With Slew-Rate Comparator
- Zero Power Detect to Prevent OVP During Light Load Conditions
- Accurate Internal V_{REF} for Tight Output Regulation
- Wide UVLO Hysteresis for Start-Up With Low V_{CC} Capacitor
- Overvoltage Protection (OVP), Open-Feedback Protection and Enable Circuits
- ± 750-mA Peak Gate Drive Current
- Low Start-Up and Operating Currents
- Minimum External Parts Required

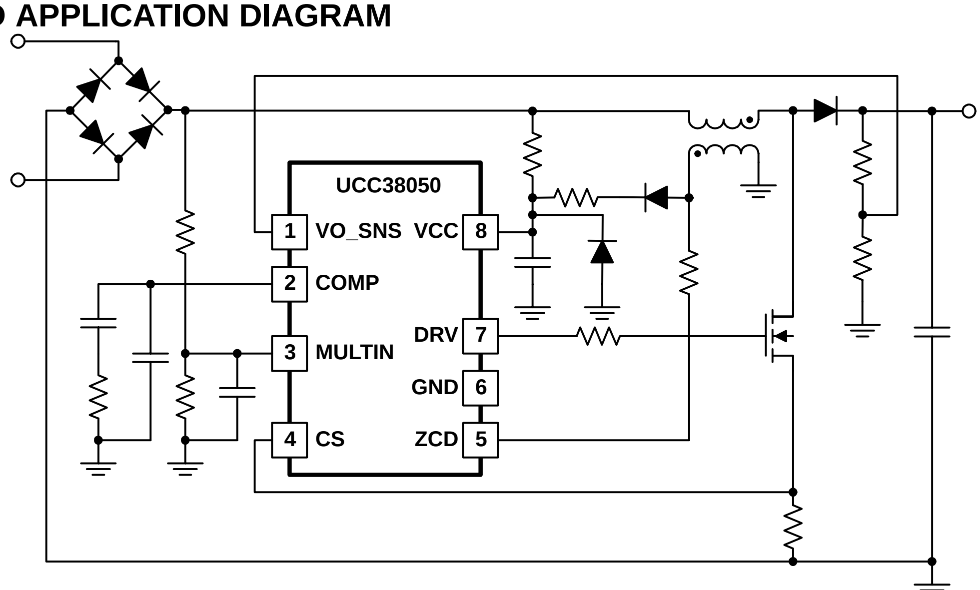
APPLICATIONS

- Switch-Mode Power Supplies for Desktops, Monitors, TVs and Set Top Boxes (STBs)
- AC Adapter Front-End Power Supplies
- Electronic Ballasts

DESCRIPTION

The UCC38050 is a PFC controller for low-to-medium power applications requiring compliance with IEC 1000-3-2 harmonic reduction standard. It is designed for controlling a boost preregulator operating in transition mode (also referred to as boundary conduction mode or critical conduction mode operation). It features a transconductance voltage amplifier for feedback error processing, a simple multiplier for generating a current command proportional to the input voltage, a current-sense (PWM) comparator, PWM logic and a totem-pole driver for driving an external FET.

SIMPLIFIED APPLICATION DIAGRAM



description (continued)

The PWM circuit is self-oscillating with the turn-on being governed by an inductor zero-current detector (ZCD pin) and the turn-off being governed by the current-sense comparator. Additionally, the controller provides features such as peak current limit, default timer, overvoltage protection (OVP) and enable.

The UCC38050, while being pin compatible with other industry controllers providing similar functionality, offers many feature enhancements and tighter specifications, leading to an overall reduction in system implementation cost. The system performance is enhanced by incorporation of zero power detect function which allows the controller output to shut down at light load conditions without running into overvoltage. The device also features innovative slew rate enhancement circuits which improve the large signal transient performance of the voltage error amplifier. The low start-up and operating currents of the device results in low power consumption and ease of start-up. Highly accurate internal bandgap reference leads to tight regulation of output voltage in normal and OVP conditions, resulting in higher system reliability. The undervoltage lockout circuit, with its high start-up voltage and wide hysteresis, also facilitates quicker and easier start-up with a smaller V_{CC} capacitance. The enable comparator ensures that the controller is off if the feedback sense path is broken or if the input voltage is very low.

Devices are available in either the industrial temperature range of –40°C to 105°C (UCC28050) or commercial temperature range of 0°C to 70°C (UCC38050). Package offerings are 8-pin SOIC (D) or 8-pin PDIP (P) packages.

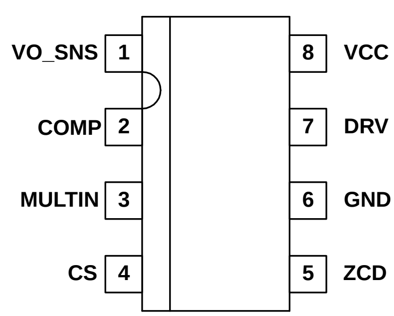
ORDERING INFORMATION

$T_A = T_J$	Packaged Devices	
	SOIC-8 (D)	PDIP-8 (P)
–40°C to 105°C	UCC28050D	UCC28050P
0°C to 70°C	UCC38050D	UCC38050P

† D (SOIC-8) package is available taped and reeled. Add R suffix to device type (e.g. UCC38050DR) to order quantities of 2,500 devices per reel.

connection diagram

D or P PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}	20 V, internally clamped
Input current into V_{CC} clamp, I_{DD}	30 mA
DRV gate drive current (peak), I_{DRV}	± 750 mA
Input voltage VO_SNS, MULTIN, CS pins	5 V
Maximum negative voltage VO_SNS, MULTIN, DRV, CS	–0.5 V
Input current for ZCD pin clamps	± 10 mA
Power dissipation at T_A = 25°C (D package)	650 mW
Power dissipation at T_A = 25°C (P package)	1 W
Junction operating temperature, T_J	–55°C to 150°C
Storage temperature, T_{stg}	–65°C to 150°C
Lead temperature (soldering, 10 sec.), T_{sol}	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

electrical characteristics T_A = 0 C to 70 C for the UCC38050, –40°C to 105°C for the UCC28050, T_A = T_J, VCC = 12 V.

supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} operating voltage				18	V
Shunt voltage	I_{VCC} = 25 mA	18	19	20	V
Supply current, off	V_{CC} = V_{CC} turn–on threshold –300 mV		75	125	µA
Supply current, disabled	VO_SNS = 0.5 V		2	4	
Supply current, on	75 kHz, C_L = 0 nF		4	6	mA
Supply current, dynamic operating	75 kHz, C_L = 1 nF		5	7	

UVLO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} turn-on threshold		15.4	15.8	16.4	
V_{CC} turn-off threshold		9.4	9.7	10.0	V
UVLO hysteresis		5.8	6.3	6.8	

voltage amplifier (VO_SNS)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage (V_{REF})	UCC38050		2.46	2.50	2.54	V
	UCC28050		2.45	2.50	2.55	V
Input bias current					0.5	µA
V_{COMP} high		VO_SNS = 2.1 V	4.5		5.5	V
V_{COMP} low		VO_SNS = 2.55 V		1.80	2.45	V
g_M		T_J = 25 °C, V_{COMP}= 3.5 V	60	90	130	µS
Source current		VO_SNS = 2.1 V, V_{COMP}= 3.5 V	–0.2	–1.0		mA
Sink current		VO_SNS = 2.7 V V_{COMP}= 3.5 V	0.2	1.0		mA

electrical characteristics T_A = 0 C to 70 C for the UCC38050, –40°C to 105°C for the UCC28050, $T_A = T_J$, VCC = 12 V.

over voltage protection / enable

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over voltage reference		VREF + 0.165	VREF + 0.190	VREF + 0.210	V
Hysteresis		175	200	225	mV
Enable threshold		0.62	0.67	0.72	V
Enable hysteresis		0.05	0.10	0.20	V

multiplier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier gain constant (k)	V_{MULTIN} = 0.5 V, COMP = 3.5 V	0.43	0.65	0.87	1/V
Dynamic input range, V_{MULTIN} INPUT		0 to 2.5	0 to 3.5		V
Dynamic input range, COMP INPUT		2.5 to 3.8	2.5 to 4.0		V
Input bias current, MULTIN			0.1	1.0	μA

zero power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero power comparator threshold(1)	Measured on V_{COMP}	2.1	2.3	2.5	V

zero current detect

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input threshold (rising edge) (1)		1.5	1.7	2.0	V
Hysteresis(1)		250	350	450	mV
Input high clamp	I = 3 mA		5	6	V
Input low clamp	I = –3 mA	0.30	0.65	0.90	V
Restart time delay		200	400		μs

current sense comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current	CS = 0 V		0.1	1.0	μA
Input offset voltage(1)		–10		10	mV
Delay to output	CS to DRV		300	450	ns
Maximum current sense threshold voltage		1.55	1.70	1.80	V

PFC gate driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GT1 pull up resistance	I_{OUT} = –125 mA		5	12	Ω
GT1 pull down resistance	I_{OUT} = 125 mA		2	10	Ω
GT1 output rise time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		25	75	ns
GT1 output fall time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		10	50	ns

(1) Ensured by design. Not production tested.

pin descriptions

VO_SNS (Pin 1): This pin senses the boost regulator output voltage through a voltage divider. Internally, this pin is the inverting input to the transconductance amplifier (with a nominal value of 2.5 V) and also is input to the OVP comparator. Additionally, pulling this pin below 0.50 V turns off the output switching, ensuring that the gate drive is held off while the boost output is pre-charging and also ensuring no runaway if feedback path is open.

COMP (Pin 2): Output of the transconductance error amplifier. Loop compensation components are connected between this pin and ground. The output current capability of this pin is 10-µA under normal conditions, but increases to about 1-mA when the differential input is greater than the specified values in the specifications table. This voltage is one of the inputs to the multiplier, with a dynamic input range of 2.5 V to 3.8 V. During zero power or overvoltage conditions, this pin goes below 2.5 V nominal. When it goes below 2.3 V, the zero power comparator is activated which prevents the gate drive from switching.

MULTIN (Pin 3): This pin senses the instantaneous boost regulator input voltage through a voltage divider. The voltage acts as one of the inputs to the internal multiplier. Recommended operating range is 0 V to 2.5 V at high line.

CS (Pin 4): This pin senses the instantaneous switch current in the boost switch and uses it as the internal ramp for PWM comparator. The internal circuitry filters out switching noise spikes without requiring external components. In addition, an external R-C filter may be required to suppress the noise spikes. An internal clamp on the multiplier output terminates the switching cycle if this pin voltage exceeds 1.7 V. Additional external filtering may be required. CS threshold is approximately equal to:

$$V_{CS} \cong 0.67\ (COMP - 2.5\ V)\left(MULTIN + V_{OFFSET}\right)$$

V_{OFFSET} is approximately 75 mV to improve the zero crossing distortion.

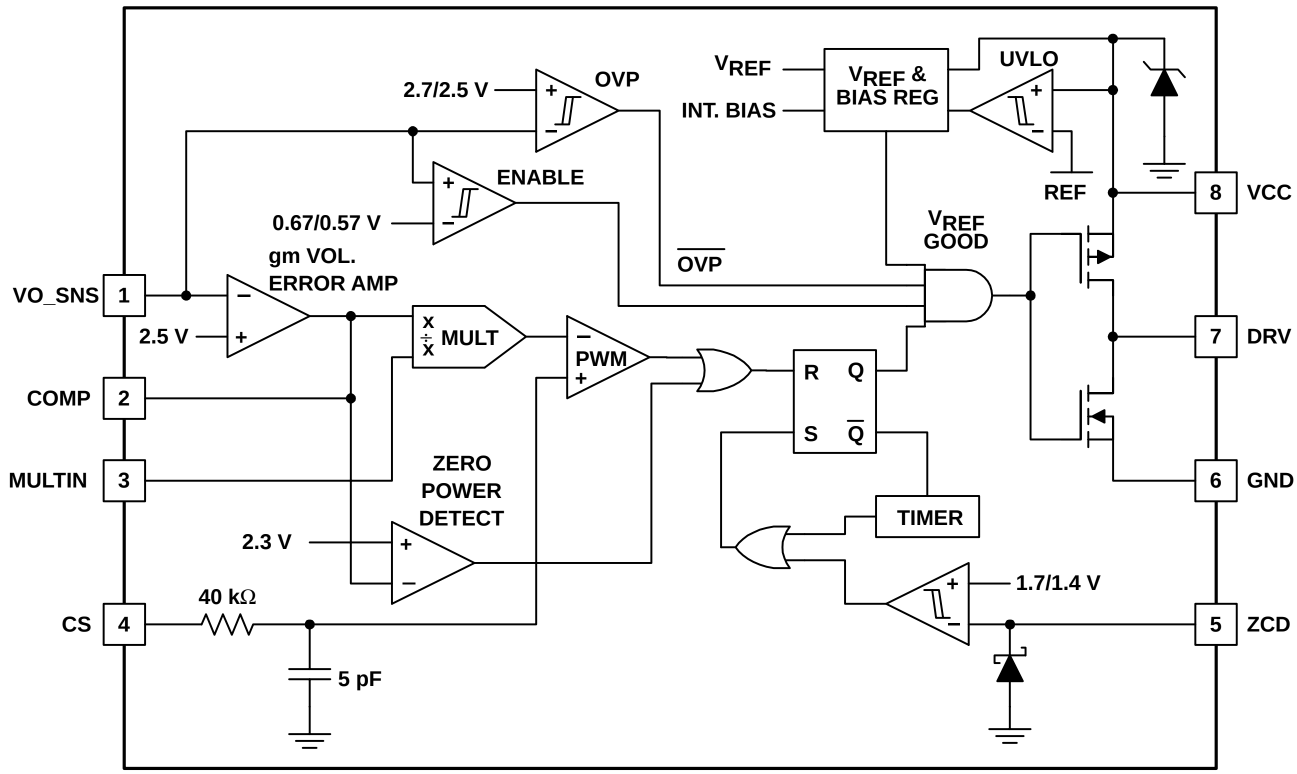
ZCD (Pin 5): This pin is the input for the zero current detect comparator. The boost inductor current is indirectly sensed through the bias winding on the boost inductor. The ZCD pin input goes low when the inductor current reaches zero and that transition is detected. Internal active voltage clamps are provided to prevent this pin from going below ground or too high. If zero current is not detected within 400 µs, a reset timer sets the latch and gate drive.

GND (Pin 6): The chip reference ground. All bypassing elements are connected to ground pin with shortest loops feasible.

DRV (Pin 7): The gate drive output for an external boost switch. This output is capable of delivering up to 750-mA peak currents during turn-on and turn-off. An external gate drive resistor may be needed to limit the peak current depending on the V_{CC} voltage being used. Below the UVLO threshold, the output is held low.

VCC (Pin 8): The supply voltage for the chip. This pin should be bypassed with a high-frequency capacitor (greater than 0.1-µF) and tied to GND. Wide UVLO hysteresis allows use of lower value supply capacitor on this pin.

block description



UDG–02008

UVLO and reference block

This block generates a precision reference voltage used to obtain tightly controlled UVLO threshold. In addition to generating a 2.5-V reference for the non-inverting terminal of the g_M amplifier, it generates the reference voltages for blocks such as OVP, enable, zero power and multiplier. An internal rail of 7.5 V is also generated to drive all the internal blocks.

error emplifier

The voltage error amplifier in UCC38050 is a transcoductance amplifier with a typical transconductance value of 90 µS. The advantage in using a transconductance amplifier is that the inverting input of the amplifier is solely determined by the external resistive-divider from the output voltage and not the transient behavior of the amplifier itself. This allows the VO_SNS pin to be used for sensing over voltage conditions.

The sink and source capability of the error amplifier is approximately 10 µA during normal operation of the amplifier. But when the VO_SNS pin voltage is beyond the normal operating conditions (VO_SNS >1.05 × V_{REF}, VO_SNS < 0.88 × V_{REF}), additional circuitry to enhance the slew-rate of the amplifier is activated. Under these conditions, the amplifier can typically sink or source currents in excess of 1 mA. This helps in quickly slewing the compensation capacitor connected at the amplifier output (COMP). This prevents the output voltage from drifting too high or low, which would happen if the compensation capacitor were to be slewed by the normal slewing current of 10 µA.

block description (continued)

zero current detection and re-start timer blocks

When the boost inductor current becomes zero, the voltage at the power MOSFET drain end falls. This is indirectly sensed with a secondary winding that is connected to the ZCD pin. The internal active clamp circuitry prevents the voltage from going to a negative or a high positive value. The clamp has the sink and source capability of 10 mA. The resistor value in series with the secondary winding should be chosen to limit the ZCD current to less than 10 mA. The rising edge threshold of the ZCD comparator can be as high as 2.0 V. The auxiliary winding should be chosen such that the positive voltage (when the power MOSFET is off) at the ZCD pin is in excess of 2.0 V.

The restart timer attempts to set the gate drive high in case the gate drive remains off for more than 400 µs nominally. The minimum guaranteed time period of the timer is 200 µs. This translates to a minimum switching frequency of 5 kHz. In other words, the boost inductor value should be chosen for switching frequencies greater than 5 kHz.

enable block

The gate drive signal is held low if the voltage at the VO_SNS pin is less than 0.67 V which translates to a output voltage of about 115 V. This feature can be used to disable the converter by pulling VO_SNS below 0.5 V (overcoming hysteresis). If the output feedback path is broken, VO_SNS is pulled to ground and the output is disabled to protect the power stage.

zero power block

When the output of the g_M amplifier goes below 2.3 V, the zero power comparator latches the gate drive signal low. The slew rate enhancement circuitry of the g_M amplifier that is activated during overvoltage conditions slews the COMP pin to about 2.4 V. This ensures that the zero power comparator is not activated during transient behavior (when the slew rate enhancement circuitry is enhanced).

multiplier block

The multiplier block has two inputs. One is the error amplifier output voltage (V_{COMP}), while the other is V_{MULTIN} which is obtained by a resistive divider from the rectified line. The multiplier output is approximately $0.67 \times V_{MULTIN} \times (V_{COMP}–2.5\ V)$. There is a positive offset of about 75 mV to the V_{MULTIN} signal because this improves the zero-crossing distortion and hence the THD performance of the controller in the application. The dynamic range of the inputs can be found in the electrical characteristics table.

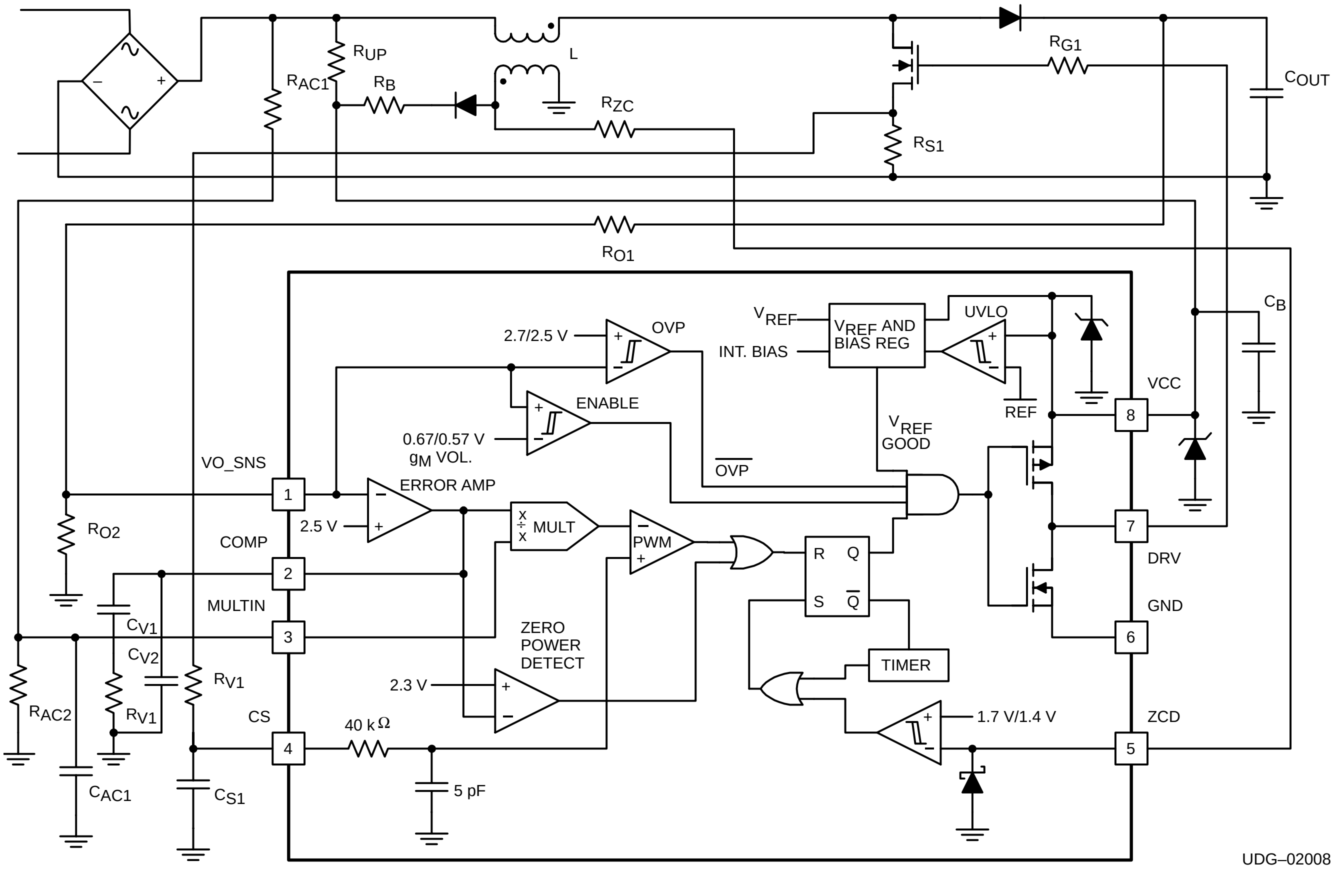
overvoltage protection (OVP) block

The OVP feature in the part is not activated under most operating conditions because of the presence of the slew rate enhancement circuitry present in the error amplifier. As soon as the output voltage reaches to about 5% above the nominal value, the slew rate enhancement circuit is activated and the error amplifier output voltage is pulled below the dynamic range of the multiplier block. This prevents further rise in output voltage.

If the COMP pin is not pulled low fast enough, and the voltage rises further, the OVP circuit acts as a second line of protection. When the voltage at the VO_SNS pin is more than 7.5% of the nominal value (>(V_{REF}+0.190)), the OVP feature is activated. It stops the gate drive from switching as long as the voltage at the VO_SNS pin is above the nominal value (V_{REF}). This prevents the output dc voltage from going above 7.5% of the nominal value designed for, and protects the switch and other components of the system like the boost capacitor.

APPLICATION INFORMATION

typical application diagram



transition mode control

The boost converter, the most common topology used for power factor correction, can operate in two modes – continuous conduction code (CCM) and discontinuous conduction mode (DCM). Transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

The CRM converter typically uses a variation of hysteretic control with the lower boundary equal to zero current. It is a variable frequency control technique that has inherently stable input current control while eliminating reverse recovery rectifier losses. As shown in Figure 1, the switch current is compared to the reference signal (output of the multiplier) directly. This control method has the advantage of simple implementation and still can provide very good power factor correction.

APPLICATION INFORMATION

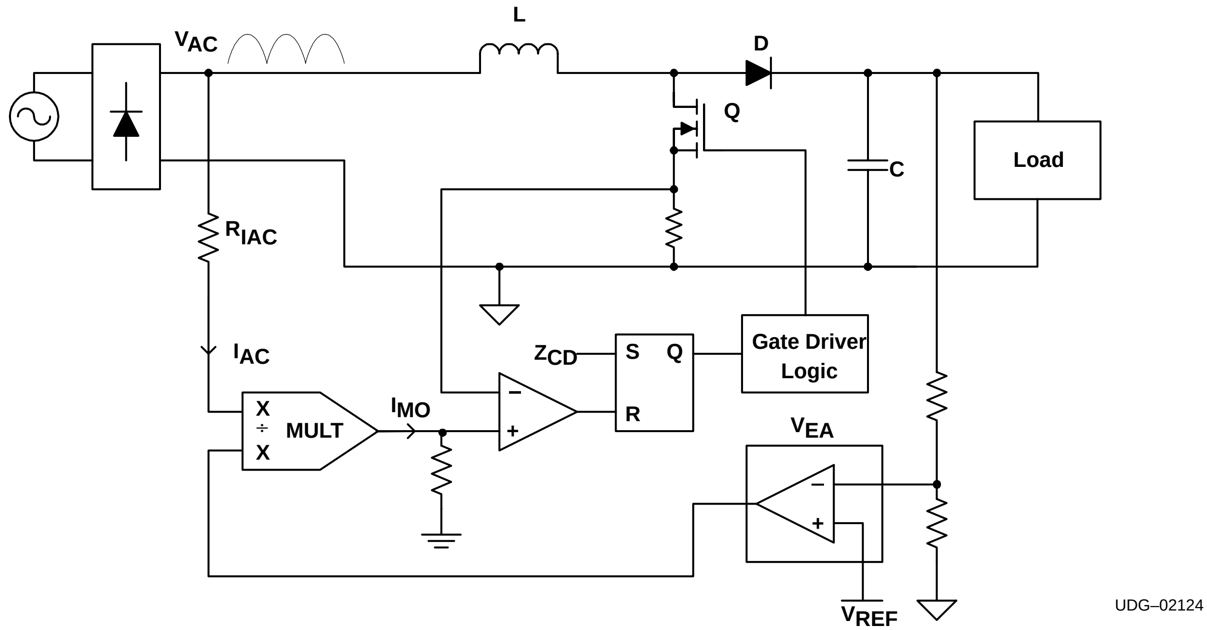
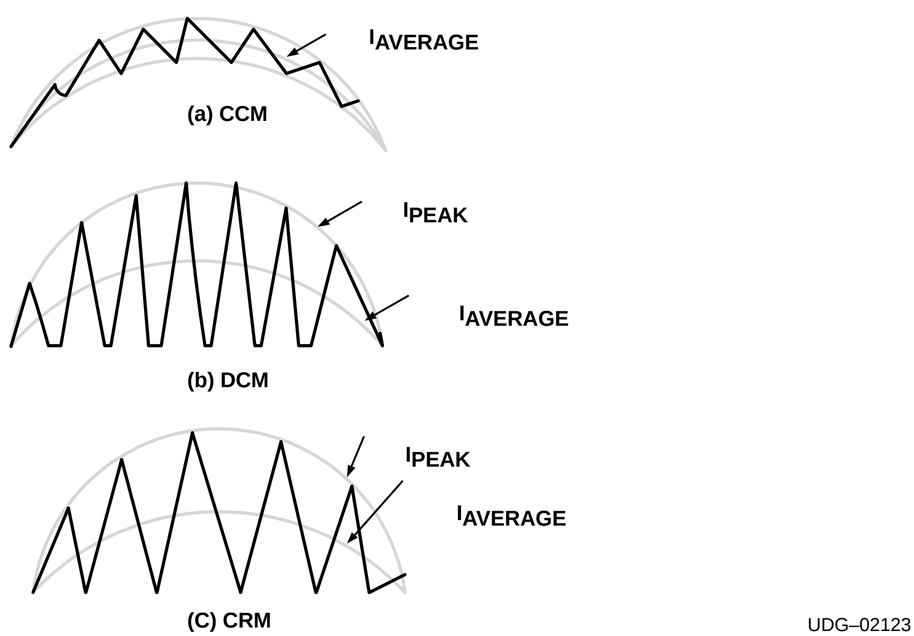


Figure 1. Basic Block Diagram of CRM Boost PFC

The power stage equations and the transfer functions of the CRM are the same as the CCM. However, implementations of the control functions are different. Transition mode forces the inductor current to operate just at the border of CCM and DCM. The current profile is also different and affects the component power loss and filtering requirements. The peak current in the CRM boost is twice the amplitude of CCM leading to higher conduction losses. The peak-to-peak ripple is twice the average current which affects MOSFET switching losses and magnetics ac losses.



Note: Operating Frequency >> 120 Hz

Figure 2. PFC Inductor Current Profiles

APPLICATION INFORMATION

For low to medium power applications up to approximately 300 W, the CRM boost has an advantage in losses. The filtering requirement is not severe and therefore is not a disadvantage. For medium to higher power applications, where the input filter requirements dominate the size of the magnetics, the CCM boost is a better choice due to lower peak currents (which reduces conduction losses) and lower ripple current (which reduces filter requirements). The main tradeoff in using CRM boost is lower losses due to no reverse recovery in the boost diode vs. higher ripple and peak currents.

design procedure

For a selected V_{OUT} and minimum switching frequency, the following equations outline the design guidelines for power stage component selection. Refer to the typical application diagram for reference designators.

inductor selection

In the transition mode control, the inductor value needs to be calculated to start the next switching cycle at zero current. The time it takes to reach zero depends on line voltage and inductance and as shown in equation (1), L determines the converter's frequency range.

$$L = \frac{V_{AC}^{2} \times \left(V_{OUT} - \sqrt{2} \times V_{AC}\right)}{2 \times F_{s(min)} \times V_{OUT} \times P_{IN}} \qquad (1)$$

where

- V_{AC} = RMS line voltage
- P_{IN} = maximum input power averaged over the ac line period

$$I_{L(peak)} = 2 \times \sqrt{2} \times \frac{P_{IN}}{V_{AC}} \qquad (2)$$

$$I_{L(rms)} = \frac{I_{L(peak)}}{\sqrt{6}} \qquad (3)$$

MOSFET selection

The main switch selection is driven by the amount of power dissipation allowable. It is important to choose a device that minimizes gate charge and capacitance and minimizes the sum of switching and conduction losses at a given frequency.

$$I_{Q(rms\_crm)} = \sqrt{\frac{1}{6} - \left(4 \times \sqrt{2}\right) \times \left(\frac{V_{AC}}{9\pi \times V_{OUT}}\right)} \times IL_{PEAK(crm)} \qquad (4)$$

$$V_{Q(max)} = V_{OUT} \qquad (5)$$

APPLICATION INFORMATION

diode selection

The effects of the reverse recovery current in the diode can be eliminated with relatively little negative impact to the system. The diode selection is based on reverse voltage, forward current, and switching speed.

$$I_{D(avg)} = I_{OUT(avg)} \tag{6}$$

$$I_{D(rms)} = I_{L(peak)} \sqrt{\frac{\sqrt{2} \times V_{AC}}{\pi \times V_{OUT}}} \tag{7}$$

$$V_{D(peak)} = V_{OUT} \tag{8}$$

capacitor selection

The hold-up time is the main requirement in determining the output capacitance. ESR and the maximum RMS ripple current rating may also be important especially at higher power levels.

$$C_{OUT(min)} = \frac{\left(2 \times P_{OUT} \times t_{HOLDUP}\right)}{\left(\left(V_{OUT}\right)^2 - \left(V_{OUT(min)}\right)^2\right)} \tag{9}$$

where:

- $V_{OUT(min)}$ = minimum regulator input voltage for operation

$$I_{C(rms)} = \sqrt{\left(I_{L(peak)}\right)^2 \times \frac{\sqrt{2} \times V_{AC}}{\pi \times V_{OUT}} - \left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + (\text{ac rms load currents})^2} \tag{10}$$

multiplier set-up

Select R_{AC1} and R_{AC2} so that their ratio uses the full dynamic range of the multiplier input at the peak line voltage yet, their values are small enough to make the effects of the multiplier bias current negligible. In order to use the maximum range of the multiplier, select the divider ratio so that V_{MULTIN} evaluated at the peak of the maximum ac line voltage is the maximum of the minimum dynamic input range of MULTIN, which is 2.5 V. Choose R_{AC1} so that it has at least 100-µA at the peak of the minimum ac operating line voltage.

$$\frac{R_{AC1}}{R_{AC2}} = \left(\frac{\sqrt{2}}{2.5} V_{AC(max)}\right) - 1 \tag{11}$$

In extreme cases, switching transients can contaminate the MULTIN signal and it can be beneficial to add capacitor C_{AC1}. Select the value of C_{AC1} so that the corner frequency of the resulting filter is greater than the lowest switching frequency. Keep in mind that the low corner frequency of this filter may compromise the overall power factor.

APPLICATION INFORMATION

sense resistor selection

The current sense resistor value must be chosen to limit the output power and it must also use the full dynamic range of the multiplier during normal steady state operation. The value of R_{S1} is thus selected for maximum power operation at low ac line voltage conditions. In order to use the full dynamic range, set the V_{SENSE} threshold as a function of the dynamic input range of V_{COMP} and the peak of the minimum MULTIN voltage.

$$R_{S1} = \frac{0.67 \times \left(COMP_{(MAX)} - COMP_{(MIN)}\right) \times \left(MULTIN_{(PEAK)@VAC(min)} - 0.075\right)}{2 \times \sqrt{2} \times \frac{P_{IN(max)}}{V_{AC(min)}}} \tag{12}$$

where:

- $COMP_{(MAX)} = 3.8\ V$
- $COMP_{(MIN)} = 2.5\ V$
- $MULTIN_{(PEAK)@VAC(min)} = \sqrt{2} \times V_{AC(min)} \left(\frac{R_{AC2}}{R_{AC2} + R_{AC1}}\right)$

If the exact value R_{S1} is not available. R_{S2} and R_{S3} can be added for further scaling. The CS pin already has an internal filter for noise due to switching transients. Additional filtering at switching transient frequencies can be achieved by adding C_{S1}.

output voltage sense design

Select the divider ratio of R_{O1} and R_{O2} to set the VO_SNS voltage to 2.5 V at the desired output voltage. The current through the divider should be at least 200 μA

APPLICATION INFORMATION

voltage loop design

How well the voltage control loop is designed directly impacts line current distortion. UCC38050 employs a transconductance amplifier (g_M amp) with gain scheduling for improved transient response (refer to Figure 14. *g_M Amplifier Output Current vs. Current Sense Voltage*). Integral type control at low frequencies is preferred here because the loop gain varies considerably with line conditions. The largest gain occurs at maximum line voltage. If the power factor corrector load is dc-to-dc switching converter, the small signal model of the controller and the power factor corrector, from COMP to PFC output voltage is given by:

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = \frac{K_1 \times \left(V_{AC}\right)^2}{V_{OUT}} \times \frac{1}{C_{OUT}(s)} \tag{13}$$

where:

- k_1 = multiplier gain = 0.65
- k_{crm} = peak to average factor = 2

A controller that has integral control at low frequencies requires a zero near the crossover frequency in order to be stable. The resulting g_M amplifer configuration is shown in Figure 3.

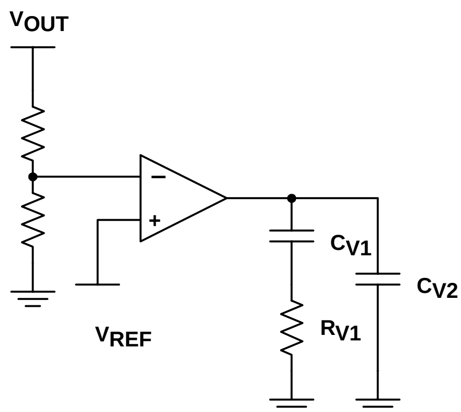


Figure 3. g_M Amplifier Configuration

The compensator transfer function is:

$$A_V = \frac{g_M}{C_{V1} + C_{V2}} \times \frac{1 + \left(R_{V1} \times C_{V1} \times s\right)}{s\left(1 + \left(R_{V1} \times \frac{\left[C_{V1} \times C_{V2}\right]}{\left[C_{V1} + C_{V2}\right]}\right) \times s\right)} \tag{14}$$

where g_M = dc transconductance gain = 100 μS

The limiting factor of the gain is usually the allowable third harmonic distortion, though other harmonics can dominate. The crossover frequency of the control loop will be much lower than twice the ac line voltage. In order to choose the compensator dynamics, determine the maximum allowable loop gain at twice the line frequency and solve for capacitor C_{V2}. This also determines the crossover frequency.

APPLICATION INFORMATION

$$C_{V2} = \left(\frac{V_{AC(max)}}{4\pi\, f_{AC}}\right)^2 \times \left(\frac{g_M \times k_1}{V_{OUT(avg)} \times R_{S1} \times k_{(crm)} \times C_{OUT(max\ loop\ gain\ @\ 2\ f_{AC})}}\right) \quad (15)$$

$$f_{CO} = \frac{V_{AC}}{\pi}\sqrt{\frac{g_M \times k_1}{C_{V2} \times V_{OUT} \times R_{S1} \times k(cmr) \times C_{OUT}}} \quad (16)$$

Select C_{V1} so that the low frequency zero is one-tenth of the crossover frequency.

$$C_{V1} = 9\, C_{V2} \quad (17)$$

Select R_{V1} so that the pole is at the crossover frequency.

$$R_{V1} = \frac{1}{2\,\pi\, f_{CO}\left(\frac{1}{C_{V1}} + \frac{1}{C_{V2}}\right)} \quad (18)$$

bias current

The bias voltage is supplied by a bias winding on the inductor. Select the turns ratio so that sufficient bias voltage can be achieved at low ac line voltage. The bias capacitor must be large enough to maintain sufficient voltage with ac line variations. Be sure to connect a 0.1-µF bypass capacitor between the VCC pin and the GND pin as close to the integrated circuit as possible. For wide line variations, a resistor, R_B, is necessary in order to permit clamping action. The bias voltage should also be clamped with an external zener diode to a maximum of 18 V.

zero current detection

The zero current detection activates when the ZCD voltage falls below 1.4 V. The bias winding can provide the necessary voltage. This pin has a clamp at approximately 5 V. Add a current limiting resistor, R_{ZC}, to keep the maximum current below 1 mA.

REFERENCE DESIGN

A reference design is discussed in *100-W Universal Line Input PFC Boost Converter Using the UCC38050,* TI Literature No. SLUU134. The UCC38050 is used for the off-line power factor corrected pre-regulator with operation over a universal input range of 85 V to 265 V with a 400 Vdc regulated output. The schematic is shown in Figure 4 and the board layout for the reference design is shown in Figure 5. Refer to the document for further details.

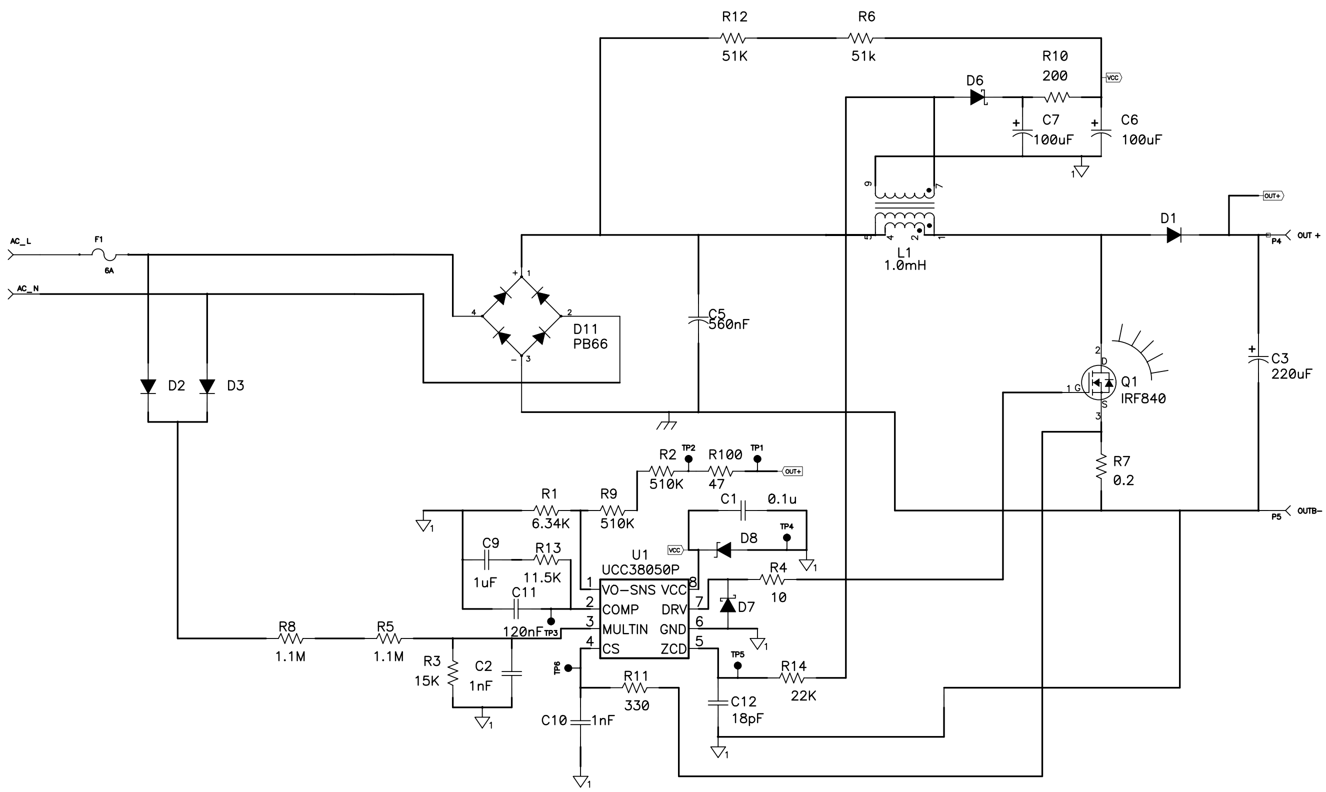


Figure 4. Universal Line Input 100-W Boost Converter Reference Design Schematic

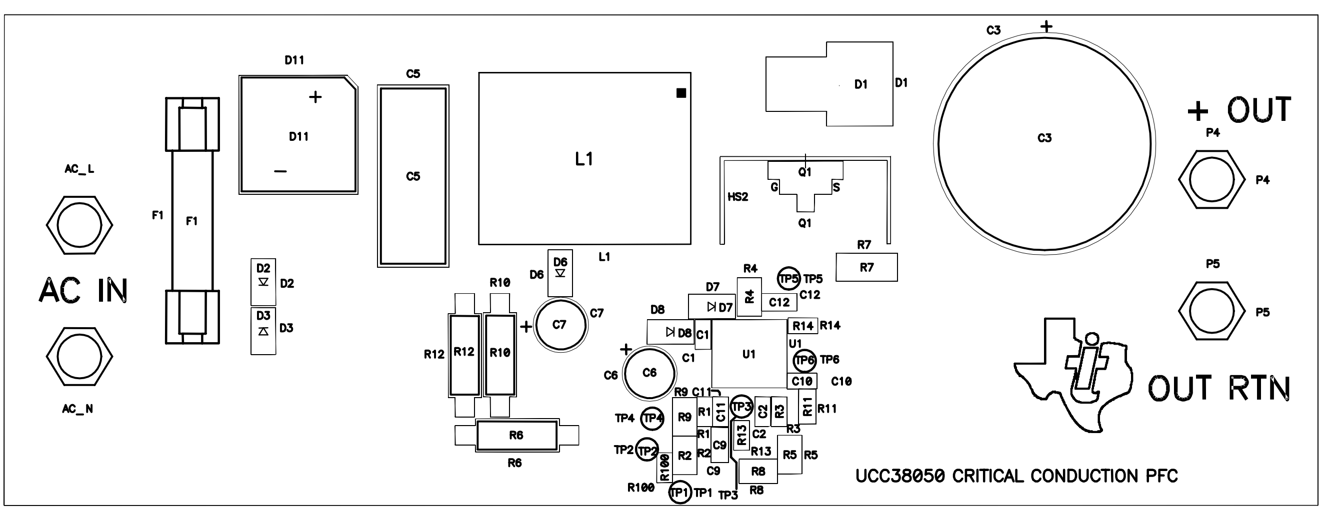


Figure 5. Reference Design Board Layout

TYPICAL CHARACTERISTICS

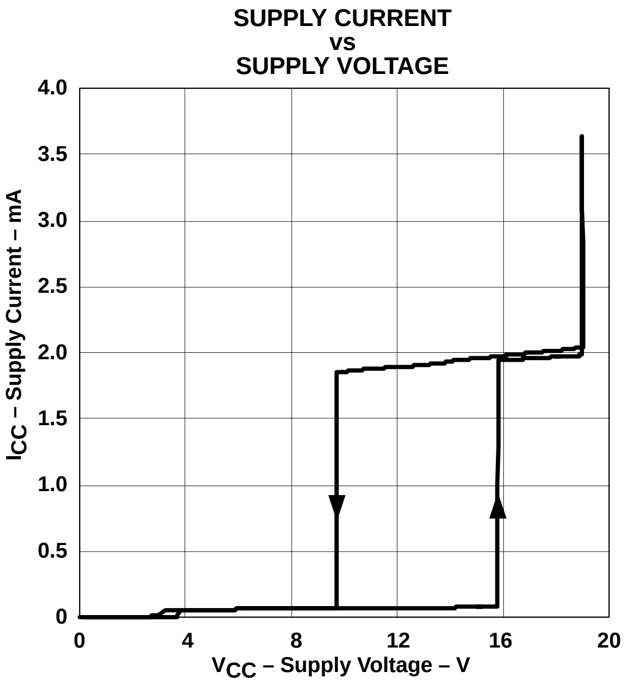
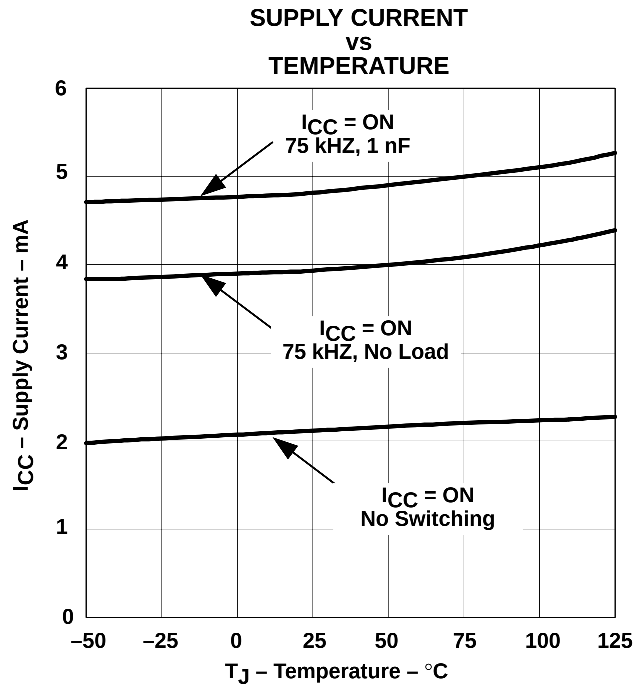


Figure 6



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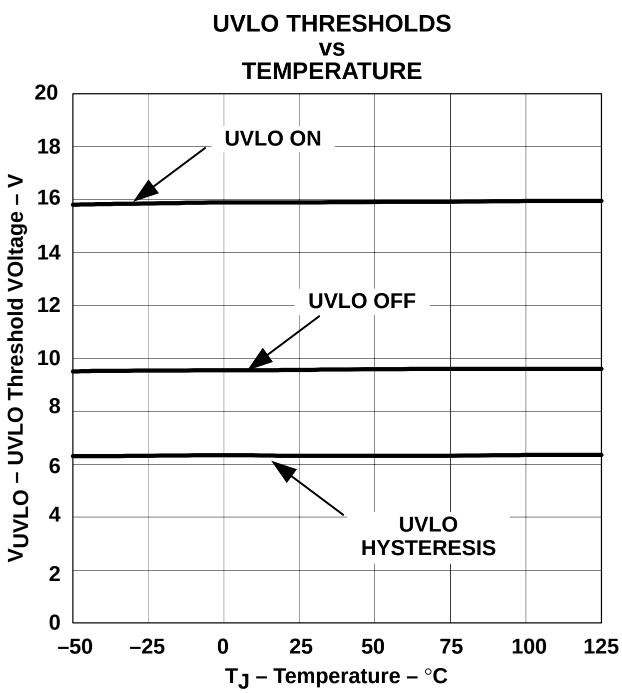


Figure 8

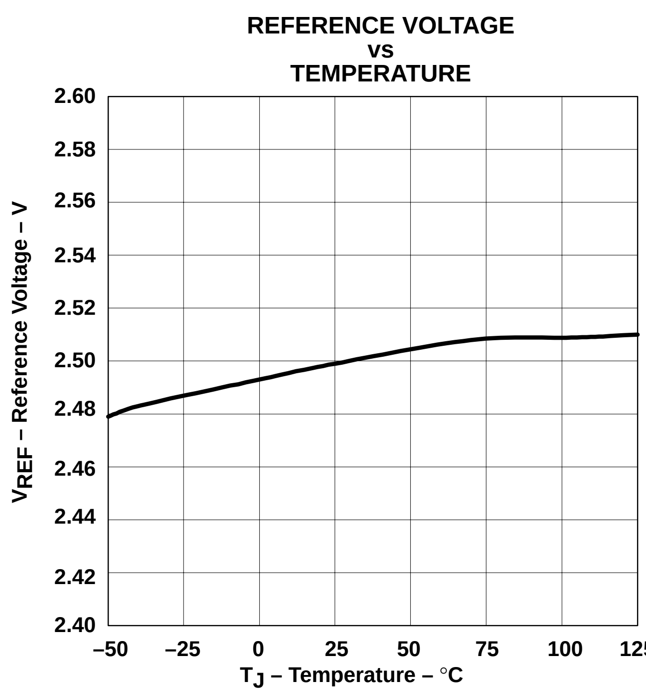


Figure 9

TYPICAL CHARACTERISTICS

CURRENT SENSE INPUT THRESHOLD vs MULTIPLIER INPUT VOLTAGE

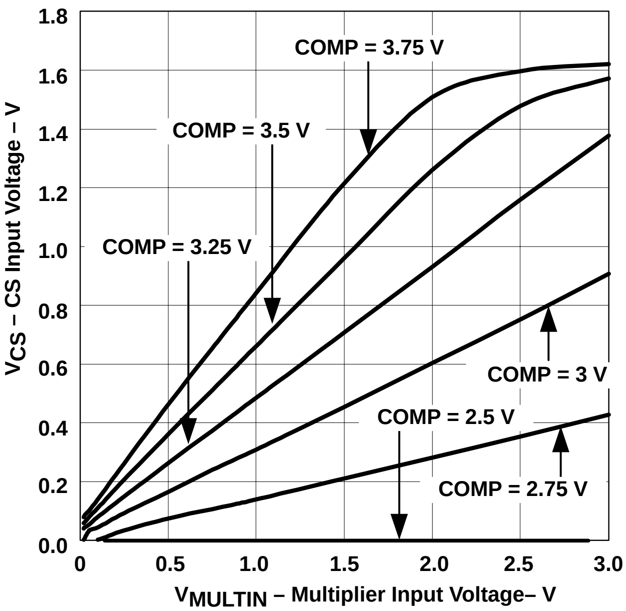


Figure 10

MAXIMUM CURRENT SENSE THRESHOLD vs TEMPERATURE

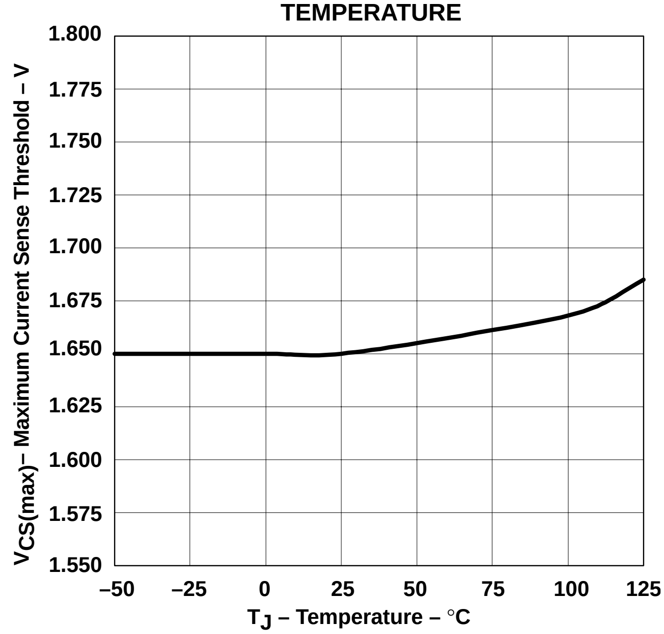


Figure 11

CS TO OUTPUT DELAY TIME vs TEMPERATURE

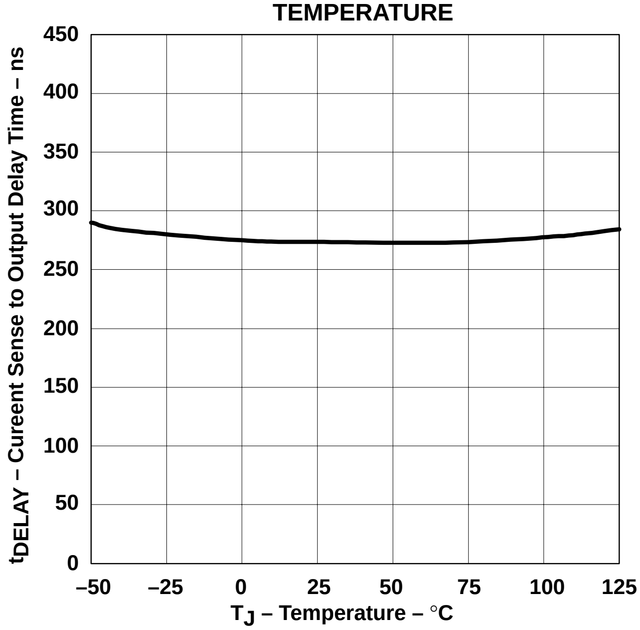


Figure 12

TRANSCONDUCTANCE vs TEMPERATURE

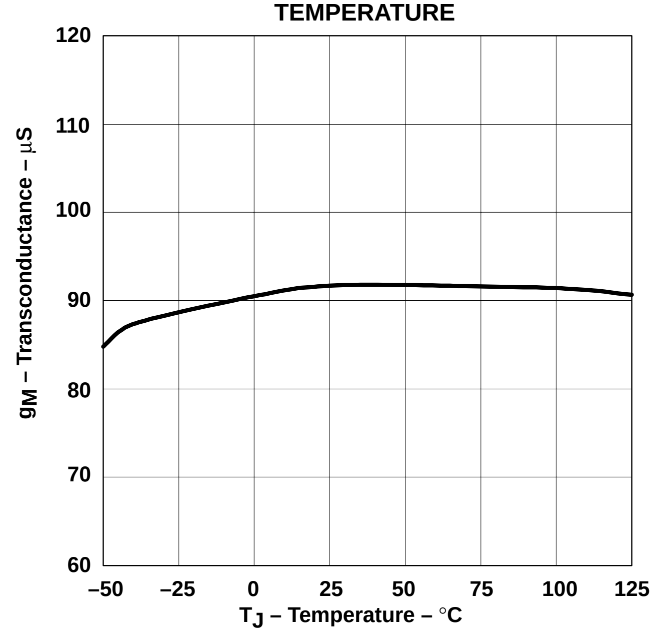


Figure 13

TYPICAL CHARACTERISTICS

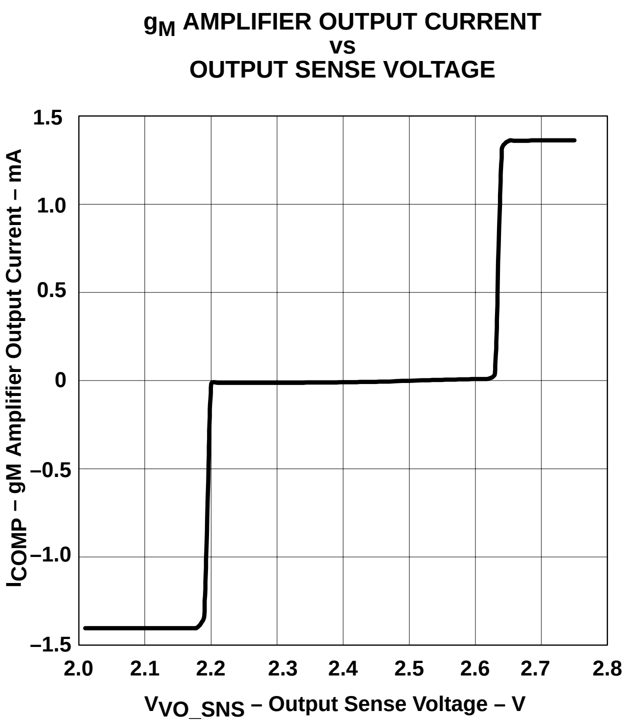


Figure 14

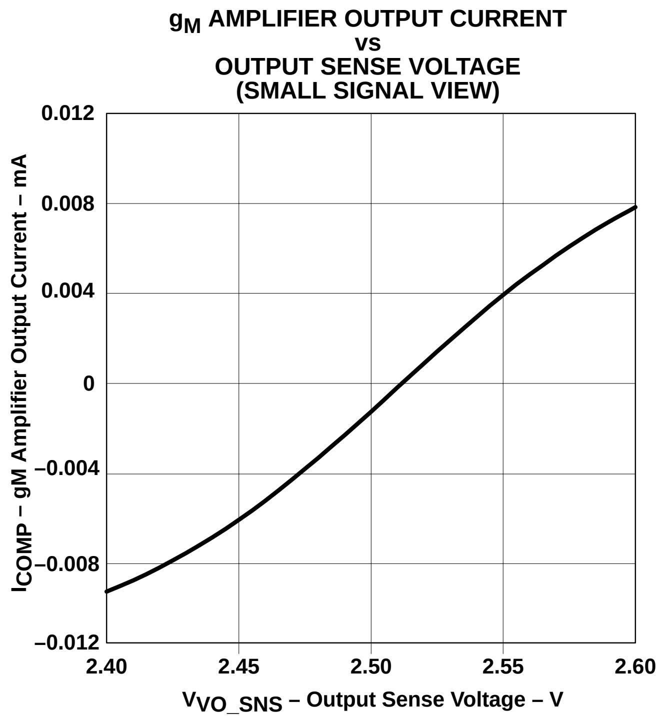


Figure 15

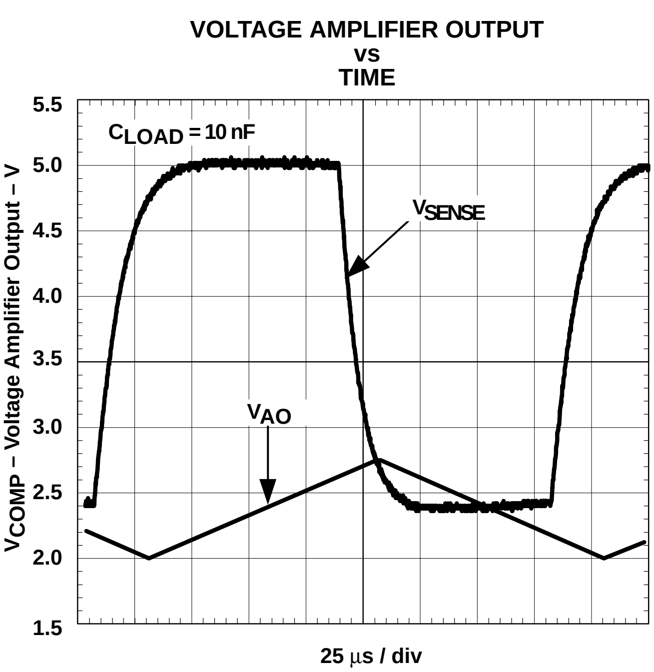


Figure 16

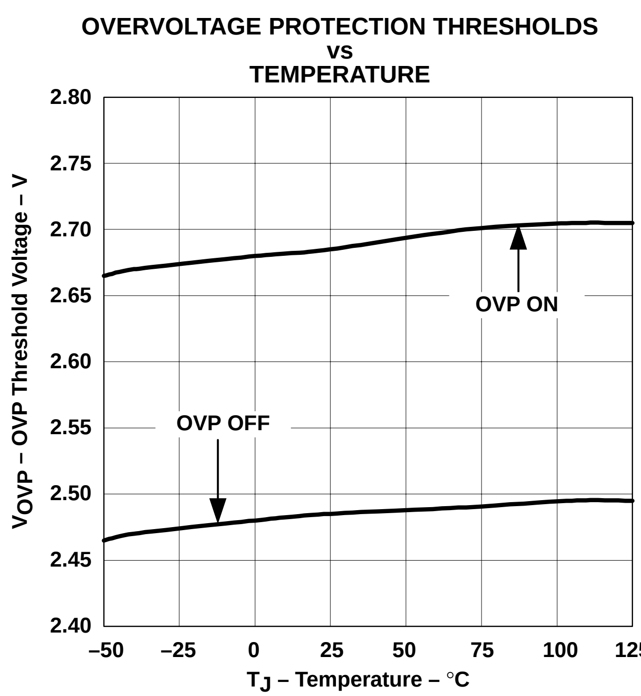


Figure 17

TYPICAL CHARACTERISTICS

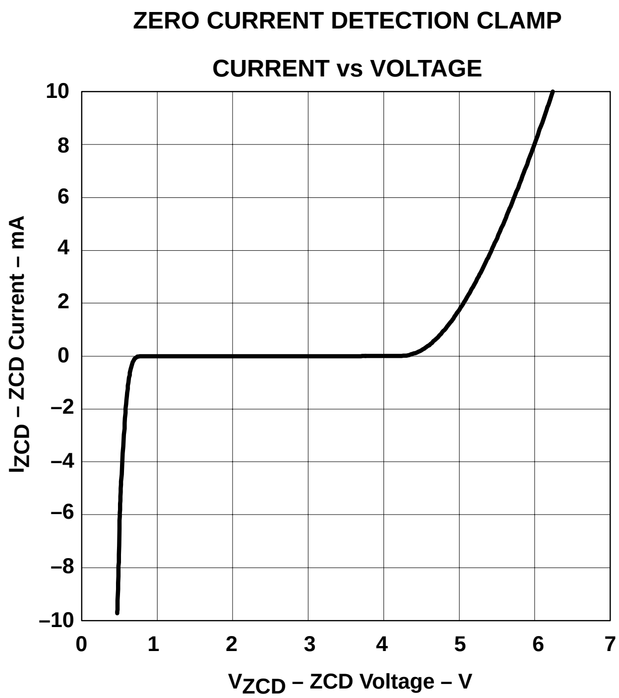


Figure 18

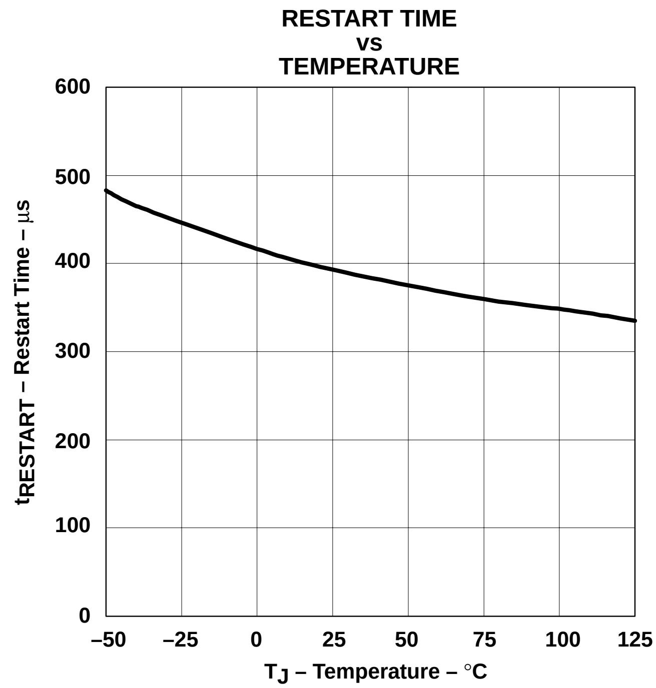


Figure 19

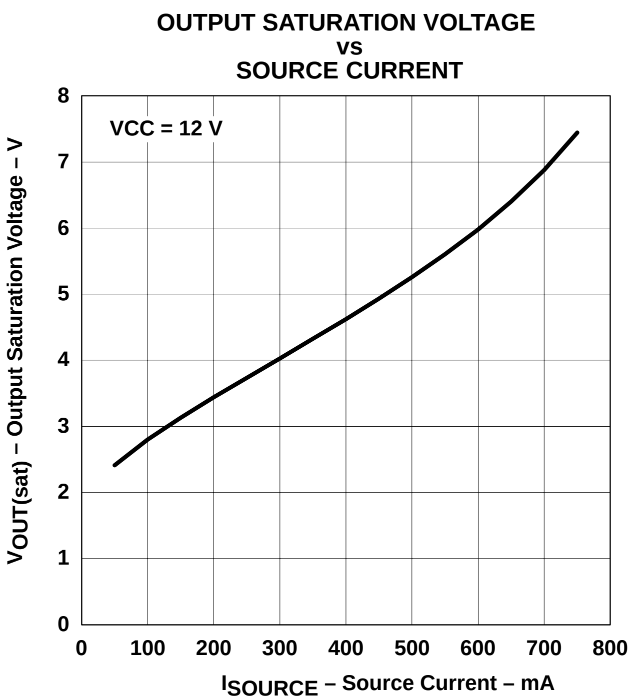


Figure 20

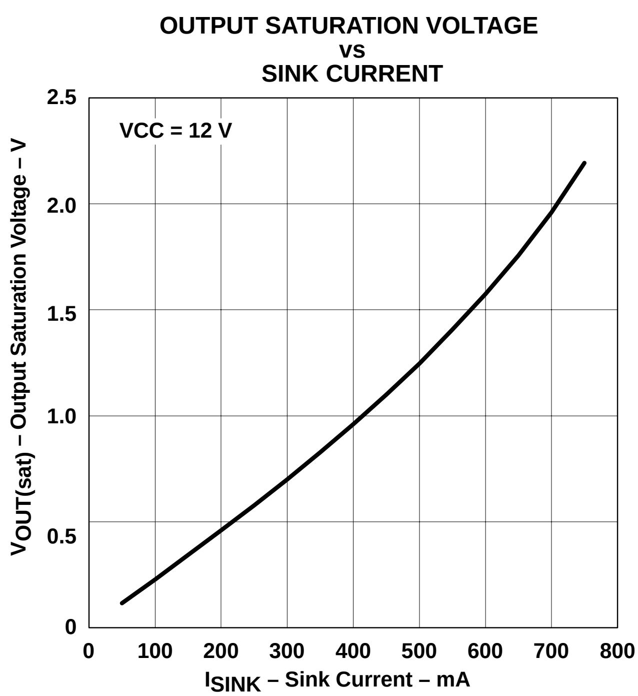
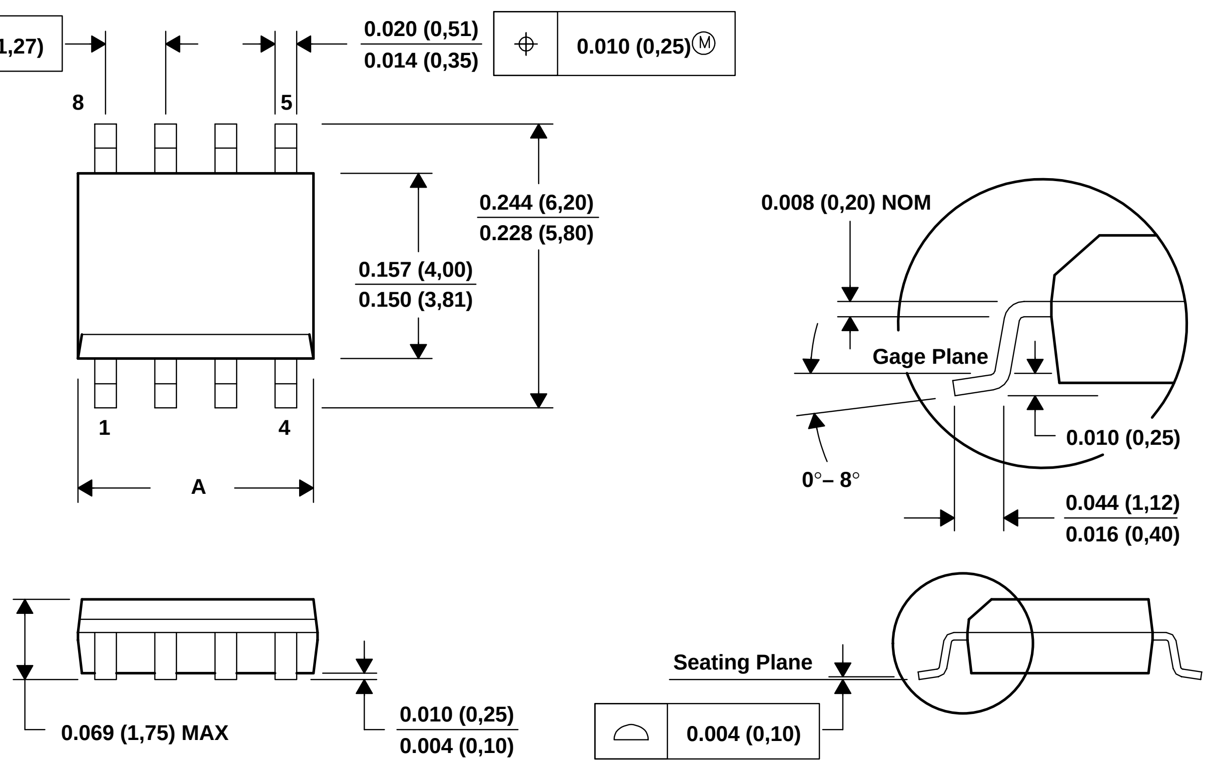


Figure 21

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



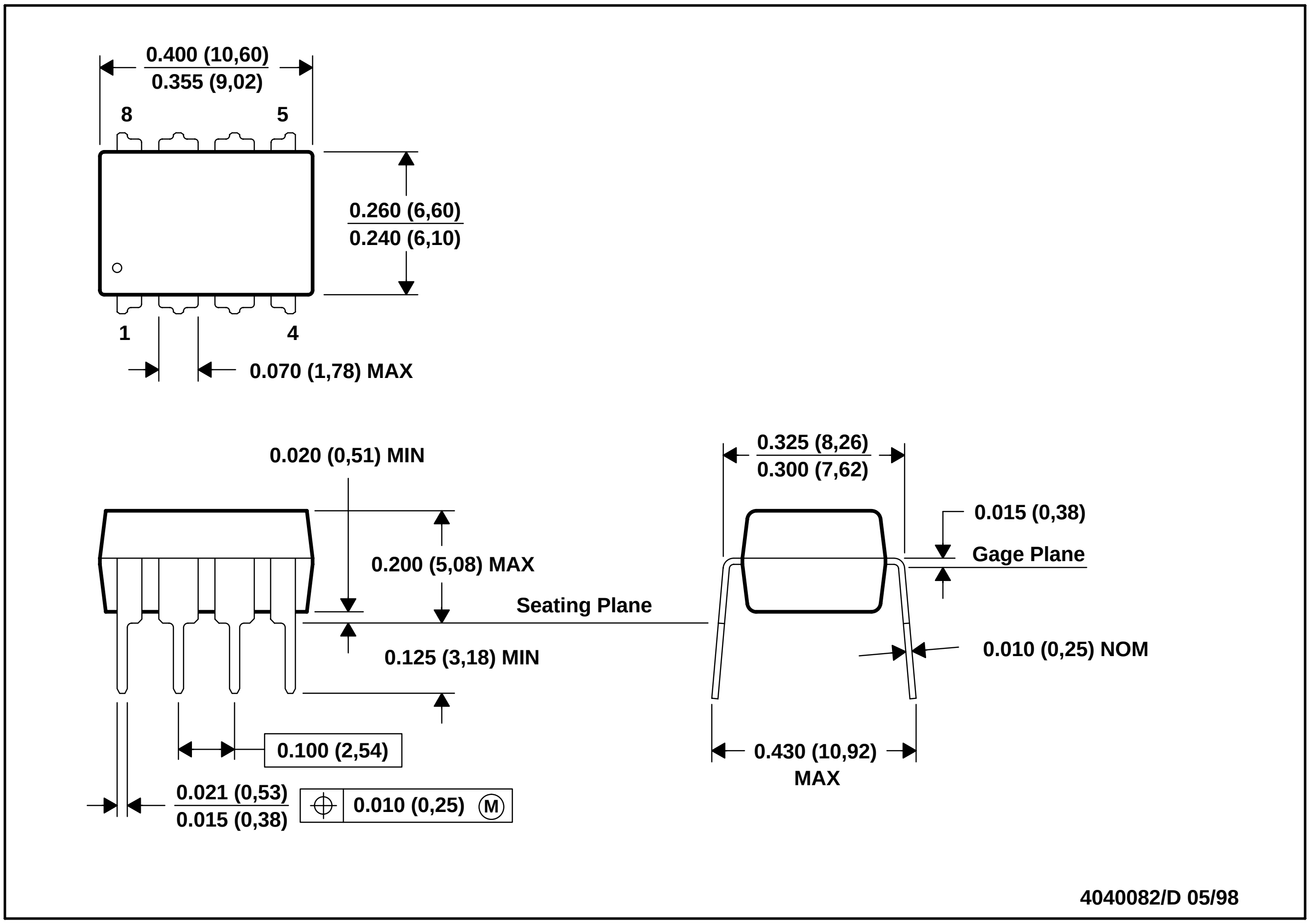
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

P (PDIP) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

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